Functional Testing

Objectives:

This section explains:

- An overview of functional testing
- What is required to execute a functional test
- Developing input/output signals
- Various functional test methods

Introduction to Functional Testing

Unlike DC testing which is mostly procedural, functional testing is unique to each device type. Voltages levels, current loading conditions, power supply settings, frequency, waveforms, IO timings, and functionality are dependent upon the characteristics of any given circuit. As a starting point for the discussion of functional test it may be best to approach the subject from a top level view, then at a later time focus on testing a specific device. This approach will enable us to understand the general issues common to all functional tests as well as the device specific issues.

Basic Terms

Functional testing introduces a few new terms: (a complete list of terminology is located in the Glossary.)

Test Vectors	A representation of the states of inputs and outputs for the various logical functions that the device is designed to perform. Input pattern data are supplied to the DUT by the test system. Output pattern data are compared against the response from the output pins of the DUT. During a functional test the test vectors are executed or applied to the DUT. In the event that the expected output data do not match the output data from the DUT then a functional failure occurs. Test vectors are also called test patterns or truth tables. Test vectors are represented as a sequence of characters which represent logical levels, and often contain instructions that are specific to the test system hardware.
Signal Format	A means of describing the wave shape of an input signal supplied by the pin electronics driver circuitry. Example: NRZ/DNRZ/RZ/RO/SBC.
Output Strobe	An output *Strobe* is the timing marker within the test system that is used as the timing reference for output signal evaluation. Many test systems offer an individual strobe marker on each tester channel, this allows each output signal to be evaluated independently.
Output Sample Time	The point in time at which the output signal of a DUT is evaluated during a functional test cycle. The comparator circuitry in the Pin Electronics qualifies the DUT output voltage to a pre–defined logic H (VOH), or logic L (VOL) reference level. The test system then makes a pass/fail decision at a specific point in time, which is defined by the strobe placement timing. Output sampling is also called output strobing.

Output Mask — A method of enabling or disabling an output comparison for a tester channel during a functional test. This can be performed on a pin-by-pin basis for each test cycle.

Functional Testing

Functional testing verifies that the DUT will correctly perform its intended logical functions. To accomplish this, test vectors or truth tables must be created that can detect faults within the DUT. The test vectors, combined with the test timing and signal formatting, make up the heart of the functional test.

All aspects of the DUT's performance must be considered when developing the functional test sequence. The exact values for the following items must be carefully examined.

Levels

VDD Min/Max	—	DUT power levels
VIL/VIH	—	input levels
VOL/VOH	—	output levels
IOL/IOH	—	output current loading
Vref	—	IOL/IOH switching point

Timing

Test Frequency	—	defines the cycle time used for test
Input signal timings	—	clocks / setups / holds / controls
Input signal formats	—	wave shapes of input signals
Output timings	—	when will outputs be sampled within cycle

Vectors

Vector sequencing	—	start / stop points within a vector file

The list above shows that the majority of the test system's resources must be used during a functional test. All functional tests consist of two distinct components, the test vector file and the instructions contained within the main test program. The test vector file represents the input and output logic states needed to test the DUT. The test program contains the information needed to control the test hardware in a manner that will create all the necessary voltages, waveforms, and timings.

As the functional test executes, the test system supplies input data to the DUT and monitors the DUT outputs on a cycle-by-cycle, pin-by-pin basis. If any output pin fails to meet the expected logic state, voltage, or timing, the result of the functional test is a failure. This type of testing is referred to as *Stored-Response* because the expected behavior of the outputs is stored in vector memory, then compared to the actual output states of the DUT.

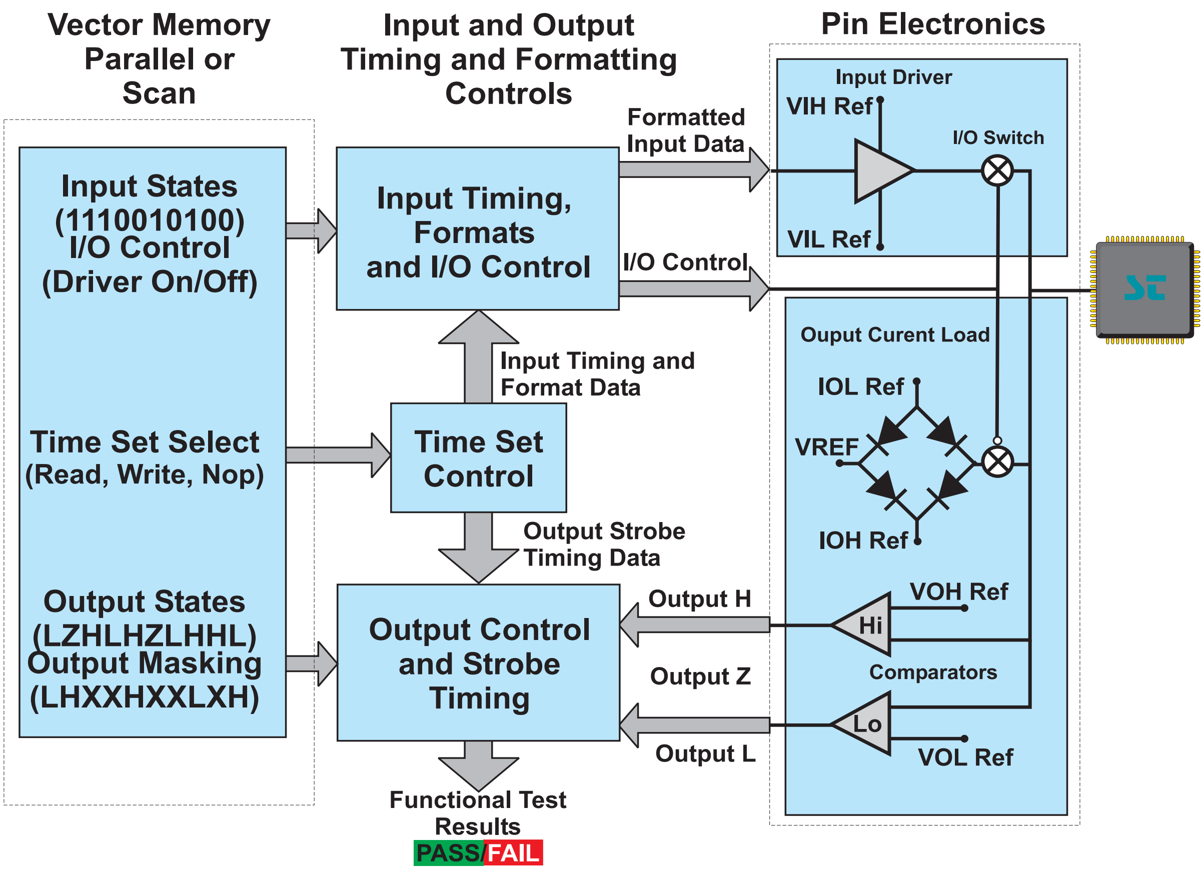


Figure 8-1 Basic Functional Testing Subsystem

Functional Subsystem

Figure 8-1 represents the basic functional subsystem of a digital tester. During functional testing input stimulation is created from vector data, signal timing, signal formatting, and input levels. DUT output signals are tested using output voltage level comparators, strobe timings, vector data, and optionally current loads. Time Set control may also be required. Review Figure 8-1 to gain an understanding of how data move through the test hardware during a functional test.

The Test Cycle

The test cycle, also called the test period, is based on the operating frequency of the device and defines the time duration of one test vector. The test cycle time can be determined by the formula:

Cycle = 1/frequency.

The start of each new cycle is called time zero or T0. When developing timing for a functional test, the first step is to determine the test cycle timing.

Input Data

Input data are created by combining:

- Test vector data (instructions or stimuli to the DUT)
- Input signal timing (signal transition points)
- Input signal formats (wave shapes)
- Input reference levels (VIL/VIH)
- Time set selections (if more than one set of timings is required)

Input data in its simplest form consists of a logic 0 or logic 1 level stored as test vector data. The voltage levels which represent a logic 0 or 1 are produced at the test head by the VIL/VIH reference voltages.

Many input signals require more complex data containing unique formats (wave shapes) and timings (edge placements). This information is contained in the main test program and is controlled through the format and timing statements of the test language.

Some test systems have shared resources which means that only a limited number of input timings, formats, and levels can be supplied by the test hardware at one time. A test system with a tester per pin architecture makes programming much easier because each pin can be programmed with unique timings, formats, and levels.

Input Signal Formats

Digital logic is controlled by applying signals to the DUT's input pins. The exact waveforms and timings needed to properly control any given circuit will be based upon each unique circuit specification. Circuits may be designed using positive or negative clock signals. Likewise, a circuit may use active low or active high control signals. Clocks and control signals pulse when active and are held at a constant level when inactive. Input data signals may simply remain unchanged at a 1 or 0 level during a cycle, they may change once during the cycle, or they may be required to pulse to a valid logic state for a specified period of time. The signal formats below enable the proper signal generation required to correctly control any digital logic circuit.

Signal formatting is very important — when properly used, formats guarantee that all AC parameters are tested to specification. Signal formats, when combined with vector data, edge timings, and input levels define the wave shape of input signals to the DUT. Figure 8-2 illustrates the most common signal formats, some ATE systems will include additional formats to help solve potential test issues, but the following examples are common to all ATE systems. Become familiar with the following formats.

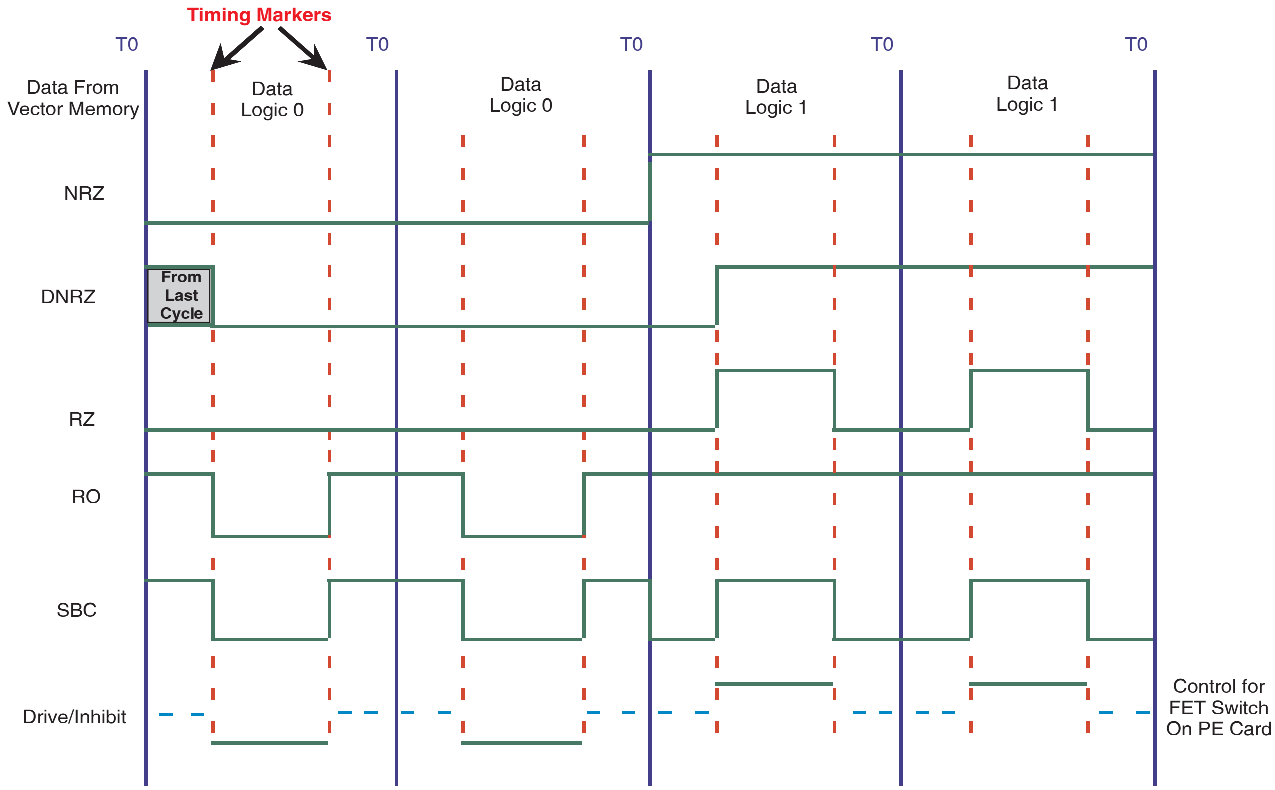


Figure 8-2 Input Signal Formats

The flowing definitions describe the functions of the most common input signal formats. Each test system seems to have a unique way of creating wave shapes. The format names and functions explained here relate to digital logic signal behavior. The test system you work with may have a different method of producing various waveforms.

NRZ — Non Return to Zero represents the actual data stored in vector memory and contains no edge timing. NRZ data changes only at the beginning of each cycle (T0). The signal stays high or low for the entire cycle. This is the most basic form of input data.

DNRZ — Delayed Non Return to Zero represents the data stored in vector memory, but the point within the cycle where the data makes a transition is defined to be a value other than the start of the cycle (T0). DNRZ data will change after a pre–defined delay period only if the vector data has changed between the current cycle and the previous cycle.

RZ — Return to Zero provides a positive pulse when vector data is logic 1 and no pulse when vector data is logic 0 (the signal remains at logic 0). RZ signals have a leading (rising) edge and a trailing (falling) edge. This signal format can provide a positive clock when vector data for the pin is logic 1. Active high signals such as CS2, as defined in the 256 X 4 Ram data sheet, will require RZ format.

RO — Return to One provides a negative pulse when vector data is logic 0 and no pulse when vector data is logic 1 (the signal remains at logic 1). RO signals have a leading (falling) edge and a trailing (rising) edge. This signal format can provide a negative clock when vector data for the pin is logic 0. Active low signals such as output enable (OE/), as defined in the 256 X 4 Ram data sheet, use RO format. RO format is often required for low true clock and control signals.

SBC Surround By Compliment can provide three edge transitions per cycle. This signal format creates a complex signal based on the vector data. It inverts the data at the start of the cycle (T0), waits a pre-defined delay, presents the actual vector data for the specified period of time, then inverts the data again for the remainder of the cycle. This signal format is the only format that will guarantee both setup and hold time in a single execution of the test vectors, and is generally used to verify signals associated with bus timing. SBC format is also known as *Exclusive-OR* (XOR) format.

Note: Drive/Inhibit is not actually considered a “format”. Drive/Inhibit allows the input driver to turn on and off within a cycle. When the driver is off the tester channel is in the high impedance state; when the driver is on the DUT input will be driven to a logic 0 or 1 depending on vector data. This format is sometimes referred to as *Z/D* and is used to control bi-directional DUT pins.

Setup and hold time parameters can be verified on test systems which do not support SBC formats by executing the test vector sequence twice. On the first execution, define setup/hold pins in RZ format to test each time a logic 1 appears in vector memory. Redefine the pins as RO to test each time a logic 0 appears in vector memory for the second vector execution.

Developing Input Signal Timings

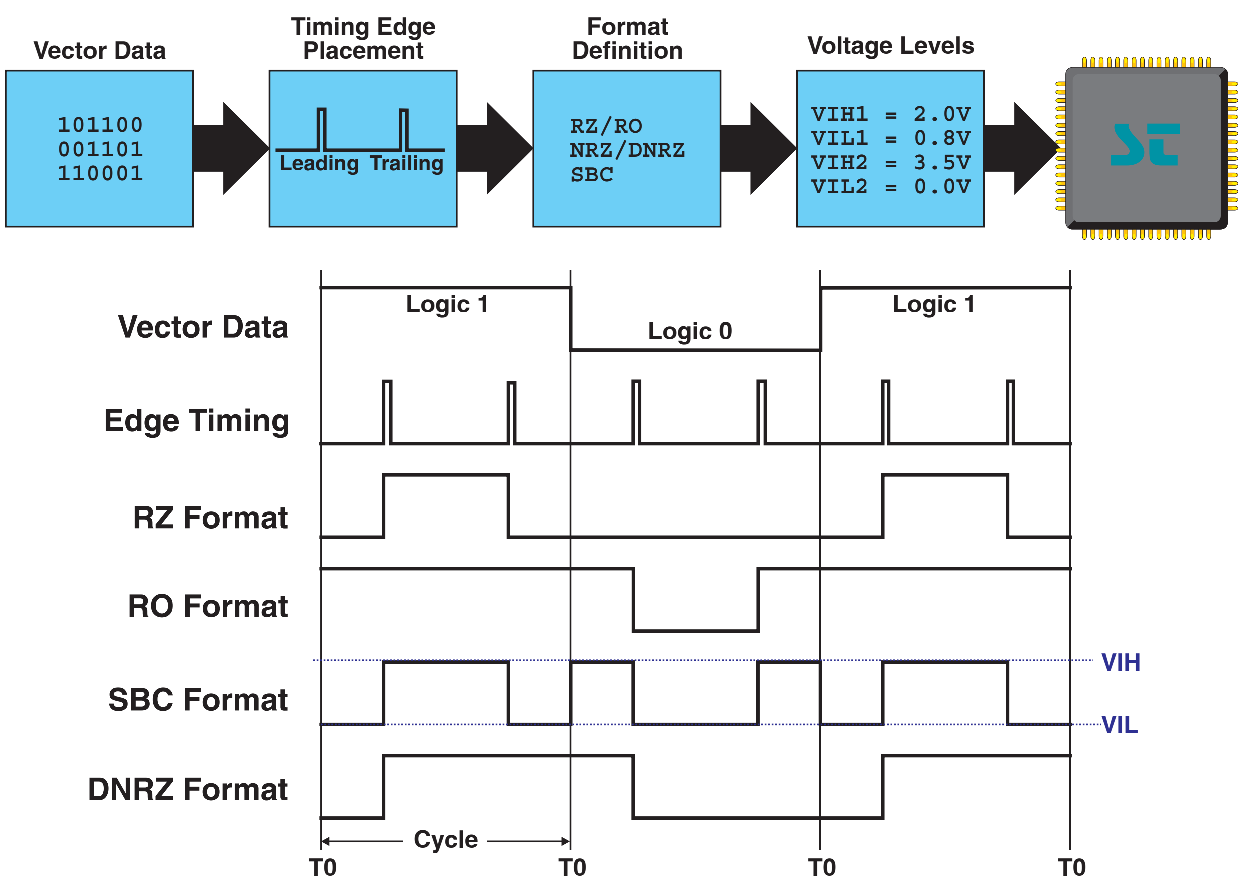


Figure 8-3 Input Signal Creation

Once the cycle time has been determined, the placement of the control signals within the cycle can be defined. There are generally two types of input signals — control signals and data signals. Data signals provide data to the device while the control signals determine the point in time when data signals will be read or latched into the internal logic of the device.

First determine the active edges of the control signals and the amount of setup and hold time required for the data signals. This information will help define the edge placement (timing) of each input signal within the test cycle.

Next determine the signal format required for each input signal. Clock signals are usually RZ (positive pulse) or RO (negative pulse) formats. Active high control signals such as CS (chip select) or READ are often RZ format. Active low control signals such as CS/ (chip select bar) or OE/ (output enable bar) are often RO format. Data signals that have a setup and hold time parameters require SBC formats. Other inputs may require NRZ or DNRZ formats.

Input signals are created by combining data from several areas within the test system. The waveform at the test head is a result of the test vector data, edge placement timing, format definition, and VIL/VIH values as shown in Figure 8-3.

Output Data

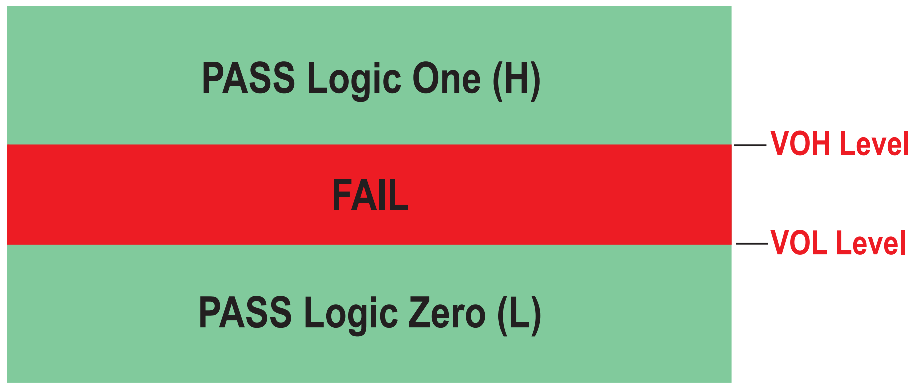
Outputs are tested by combining:

- Test vector data (expected logic states from the DUT)
- Output strobe timing (when to sample outputs within the test cycle)
- VOL/VOH (reference levels to determine output states from DUT)
- IOL/IOH (output current loading)
- Time set selections (if more than one time set is used)

Testing Outputs

During a functional test the voltage level of the output signals from the DUT are compared to the VOL and VOH reference levels by the functional comparators. An output strobe is assigned a timing value for each output pin to control the exact point within the test cycle for sampling the output voltage.

The test vectors contain the expected logic states for each pin. If the expected state is a logic zero (L), the DUT output must be equal to or less than the VOL reference level when the output strobe occurs. If the expected state is a logic high (H), the DUT output must be equal to or greater than the VOH reference level. Many test systems also have the ability to test for a high impedance state (Z) which is defined as greater than VOL and less than VOH.



Comparator logic for valid output levels

DUT Output voltage must be equal to or greater than VOH to pass a High

DUT Output voltage must be equal to or less than VOL to pass a Low

Figure 8-4 Valid Logic Level Testing

Testing Valid (L/H) Output Levels

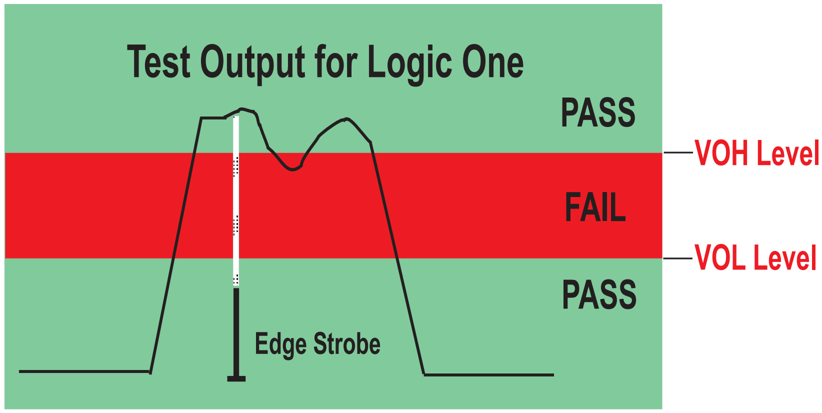
Figure 8-4 shows the pass/fail/pass relationship between the DUT output and the VOL/VOH reference values for testing valid (normal) output levels.

The output voltage produced by the DUT must be equal to or greater than the VOH reference level of the comparator to be qualified as a valid output high.

The output voltage produced by the DUT must be equal to or less than the VOL reference level of the comparator to be qualified as a valid output Low.

Output Testing using an Edge Strobe

The voltage value of a digital output signal is evaluated at a particular point in time to determine the logic state of the output. An output *Strobe* is the timing marker within the test system that is used as the timing reference for output signal evaluation. Many test systems offer an individual strobe marker on each tester channel, this allows each output signal to be evaluated independently. There are two types of strobe markers commonly available: edge and window.



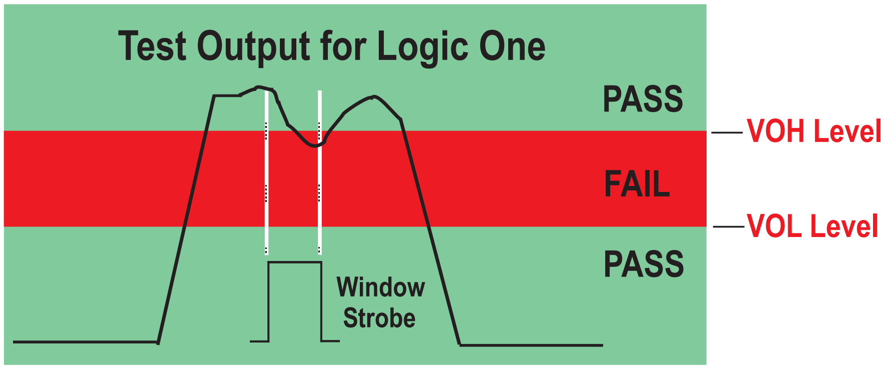
The Result of this test is a PASS
Edge Strobes are a single point in time
Pass/Fail evaluation is made only at strobe time
Strobe timings are referenced to Time Zero

Figure 8-5 Edge Strobe

Figure 8-5 shows the placement of an edge strobe and the point of output evaluation. In this example the output signal is being tested for a logic one. As shown above the output voltage is greater than the VOH reference level at the time that the edge strobe occurs. In this example the result of the test is a PASS. An edge strobe makes an evaluation at a single point in time. Edge strobes are often used in high frequency testing because they are less affected by noise or ringing of the output signal. The exact placement of the output strobe is determined from information contained in the device AC specification, but strobe timing is programmed relative to T0 (time zero of the tester cycle)

Output Testing using a Window Strobe

Figure 8-6 shows the placement of a window strobe and the duration of output evaluation. In this example the output signal is being tested for a logic one. Notice that the output voltage falls below the VOH reference level during the time that the window strobe is active, the result of this test is a FAIL. A window strobe makes the evaluation during the entire strobe width. The test will fail if the output voltage fails to correctly qualify at any point during the strobe window timing. Ringing or noise on the output signal can cause the test to fail when using a window strobe.

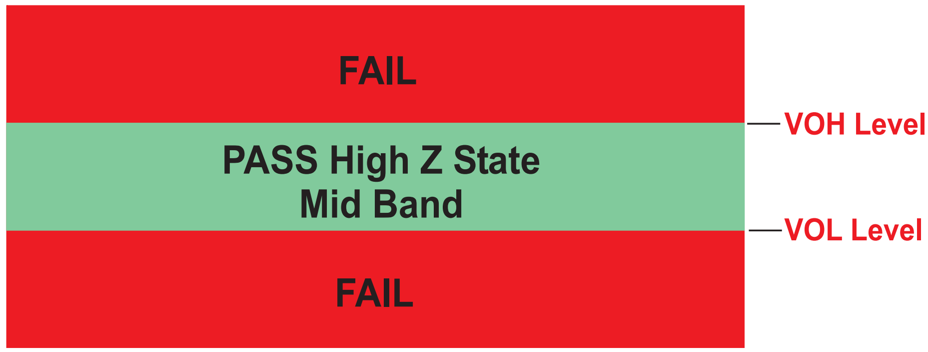


Result of this test is a **FAIL**
The Output voltage dropped below VOH level
A PASS level must be maintained during entire "Window"
Window Strobes are sensitive to noise

Figure 8-6 Window Strobe

Testing High Impedance (Z-state) Output Levels

Outputs can be functionally tested for a high impedance condition. In this type of testing, the comparator logic is inverted to expect a non-valid logic level (not 1 and not 0). A high impedance state is defined as a voltage that is greater than the VOL reference level and less than the VOH reference level (see Figure 8-7). A voltage external to the DUT is required to pull the high impedance output to a non-valid (intermediate) voltage. This is accomplished using of a load connected to a reference voltage. A reference voltage based upon the formula (VOL+VOH)/2 is often used to represent the intermediate or high-Z level. Remember, when an output enters a high impedance state, it loses the ability to supply voltage and current. A high impedance output will tend to stay at its last valid logic level unless something external to the device causes the output to change. The test system load pulls the DUT output to the specified reference voltage.



Comparator logic for High Impedance Levels

Figure 8-7 High Impedance Testing

Figure 8-7 shows the fail/pass/fail relationship between the DUT output and the VOL/VOH reference values for testing high impedance output levels.

Output Current Loading

Current loads may be applied to the DUT outputs during a functional test. Programmable current loads (also called dynamic current loads) consist of circuitry located in the pin electronics, and their voltage and current settings are defined within the test program. If the test system does not support programmable loads, resistive loads may be added to the external test hardware. Current loads apply the proper IOL and IOH currents to the outputs as the functional test executes. By applying the specified IOL/IOH currents and testing for the specified VOL/VOH voltages, the output current and voltage parameters can be verified during the execution of a functional test. This is much faster than performing the same tests using the PMU.

Developing Output Strobe Timing

Output signal transitions are often controlled by a clock or control signal edge. To fully understand this you must review the device timing diagram and determine the active edge of the clock or control signals that cause output signals to change. Determine the amount of propagation delay time needed before the output reaches a valid logic level. This point within the cycle is where the output strobe should be placed for that particular signal.

The output strobe can be a point in time or a window in time depending on the test system hardware capabilities. When the output strobe occurs the output signal for the DUT is sampled. The signal must be equal to or greater than the VOH voltage if the test vector defines the expected output as logic 1. The signal must be equal to or less than the VOL voltage if the test vector defines the expected output as logic 0.

As a general rule it is best to define test timing so that outputs transition and are tested within the same cycle. This allows propagation delays to be accurately measured without crossing test cycle boundaries. Make certain that outputs have sufficient time to propagate out before the end of the test cycle. Some device output pins take longer than others to reach their final value; testing at an increased frequency can expose propagation delay problems. Also be aware that some test systems may have limitations regarding how close an output strobe can be placed to the beginning or end of the T0 test cycle boundary.

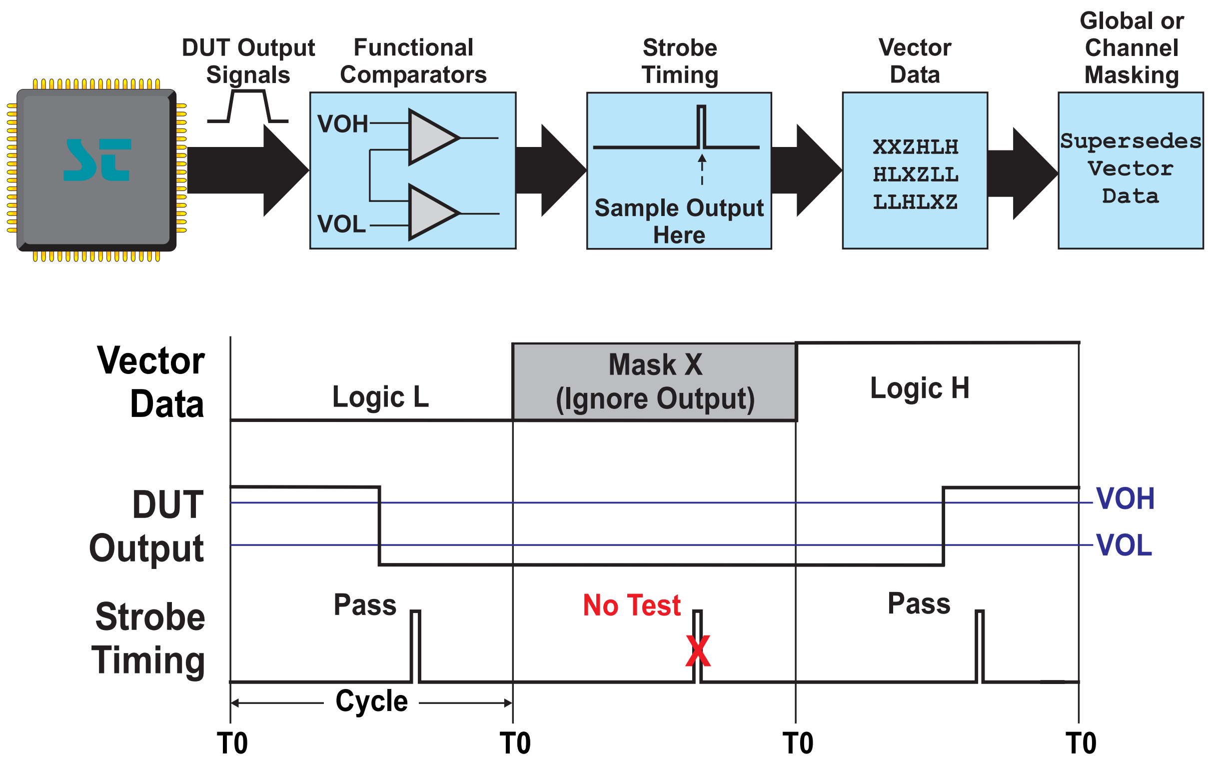


Figure 8-8 Output Signal Testing

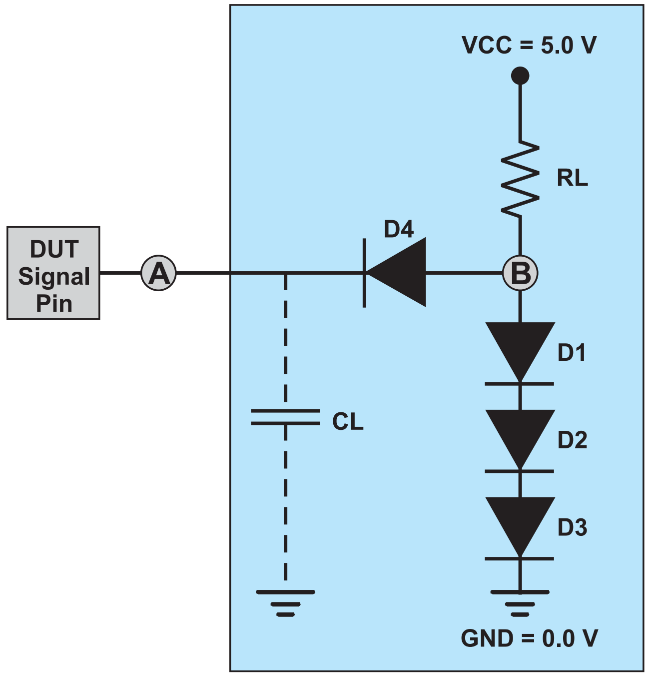
As illustrated in Figure 8-8, a combination of factors influence exactly when and how an output signal is tested:

- The vector data determine the expected logic state (L/H/Z/X).
- The VOL/VOH reference levels qualify the DUT output voltage.
- The output strobe timing defines the point within the cycle at which the output signal is evaluated.
- The output compare mask controls whether the result of the test will be used to make a pass/fail decision or if the result will be ignored. The output compare mask can be used in 2 ways. The character “x” is used to select on a pin-by-pin, cycle-by-cycle basis whether to test or ignore any given output pin. Many systems also have a Global Mask or a Master Mask which will override the data contained in vector memory.

Output Loading for AC Tests

A device specification may indicate that a current load must be placed on the output of the device when performing the AC timing tests. Loads are often resistor/diode/capacitance networks that simulate loading conditions of circuitry which will be connected to the device in its final application (e.g. in a computer or cellular telephone). In the past the type of load shown below was required when testing TTL circuits, hence the term *loadborad*. CMOS device specifications may indicate the need for some type of output loading, but the design will be different from the example below.

Examine the AC load in Figure 8-9. As a starting point VCC is set to 5.0 V and nothing is connected at point A. Under these conditions point B will be approximately 2.1 V (0.7 V dropped across each diode) and point A will also be at 2.1V. The voltage seen across RL is 2.9 V (VCC - 2.1), therefore 1.45 mA of current will flow through RL and the three diodes to ground.



RL = 2000 Ω
CL = 15 pF
Diodes = 1N3064

Figure 8-9 TTL Output Load Testing

Next, a device output driving logic 0 (0.4 V) is connected to point A. This forward biases diode D4, pulling point B to 1.1 V (0.4 V plus one 0.7 V diode drop). There is now 3.9 V across RL and the current through RL into the device output is 1.95 mA, loading the device output when driving a logic 0.

When the device output drives a logic 1 (2.4 V) D4 becomes reversed biased and eliminates the current loading effect. For this example the AC load provides a current load only for a logic 0; when the device drives a logic 1 the load is essentially removed.

Note: The test fixture may provide more capacitance than 15 pF, so for load capacitance specifications less than 20–30 pF (depends on the tester) the CL load capacitors are not physically added to the AC test load.

Vector Data

The test vector file contains the truth table that exercises the various functions the DUT is designed to perform. The vector file contains the logic states that must be applied to the DUT inputs, and also the logic states which are expected to appear on the DUT outputs. Vector data often consist of the following set of characters.

Vector Characters	Driver State	Comparator State	Pin State
0 = logic 0	driver on	comparator off	input
1 = logic 1	driver on	comparator off	input
L = logic 0	driver off	comparator on	output
H = logic 1	driver off	comparator on	output
Z = float	driver off	comparator on	output
X = don't care	driver off	comparator off	ignore

Table 8-1 Test Vector Data Example

The vector file may also contain instructions to the test system hardware. If the DUT has I/O pins (pins that act as both inputs and outputs) then the vector file must control when the input driver circuitry turns on and off. The I/O switching can occur on a cycle-by-cycle basis, changing with the DUT pin from input to output, or from output to input.

The test vectors may contain masked output pins. A mask is used to control the testing of an output pin. When a DUT output is in a known logic state it can be tested, but there may be occasions when the output is in an unknown or don't care state. A mask is used to ignore the pass/fail result of an output. Masking is generally available for each individual pin and can be selected or deselected on a cycle-by-cycle basis.

If the tester supports multiple time sets, then the vectors may contain time set information. Multiple time sets are used to change the test timing as the vectors are being executed. For example, when testing a RAM it typically takes less time to write data into the RAM than to read data from the RAM. In this case there may be one time set that contains write timing and one time set that contains read timing. The vectors will contain control statements to select the appropriate time set for the appropriate vector functions (reading or writing). Time sets can control cycle times, input timings and formats, and output strobe timings.

Executing a Functional Test

The following steps are required to execute a functional test:

1. Define VDD level
2. Define input drive and output reference levels (VIL/VIH/VOL/VOH)
3. Define output current loading (IOL/IOH/Vref)
4. Define test cycle time
5. Define input timings and formats for all input pins
6. Define output strobe timings for all output pins
7. Define start and stop locations of the pattern within vector memory
8. Execute the test

Functional Specifications

Two methods are commonly used to functionally verify device specifications. In the first method, all input, output and timing parameters are set to their worst-case conditions and the functional vector sequence is executed. This approach is fast and guarantees that the device meets the design specifications. However, if a failure occurs it is not apparent which parameter caused the failure.

An alternate approach is to test the parameters individually. For example, only set VIL/VIH to the values defined in the device specification, with other parameters relaxed. If a failure occurs, it is immediately known that the cause was either the VIL level or the VIH level. The testing continues until all parameters have been verified. This approach offers more detailed information regarding yield issues but increases test time.

Relaxed Parameters

When a parameter value is relaxed its value is adjusted in a way that will make it easier for the DUT to function properly. For example, if VIL is specified as 04 V it could be relaxed by setting the value to 0.0 V. By lowering the value of VIL it becomes easier for the DUT to detect the input voltage as a logic 0. To relax inputs, lower the VIL levels and raise the VIH levels. To relax outputs, set both VOL and VOH to VDD/2, the comparators will then sense any output voltage below VDD/2 as a logic 0 and any output voltage above as a logic 1. *Note:* output comparator levels cannot be relaxed when testing for “Z” state levels. To relax timing values, reduce the test rate, increase setup and hold times, and increase output propagation delays.

Timing Parameters

AC timing specifications are verified by presenting the appropriate waveforms to the device under test. Setup times, hold times, minimum pulse widths, and propagation delays must be tested. In some cases it may be possible to apply all worst-case conditions at once and guarantee that the device meets the complete device specification with only one test execution. Complex functional timings may require several test iterations with different conditions to guarantee the complete device specifications.

MIN/MAX Voltages

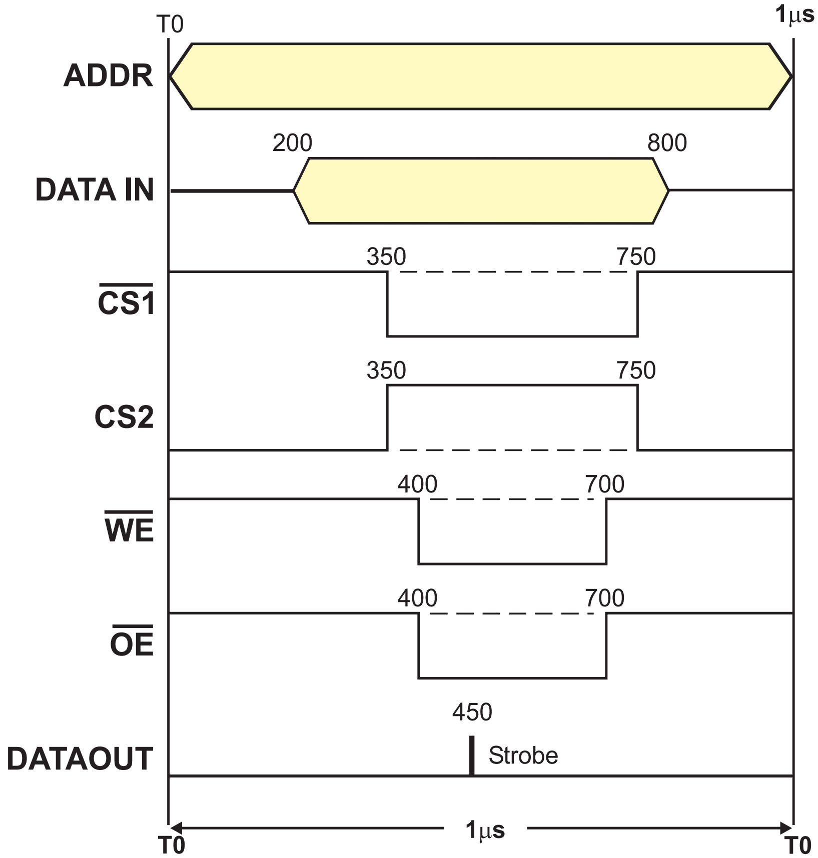
Device specifications often define the operating voltage range of VDD. For instance VDD=3.0 V ±10% indicates that for a VDD of 3.0 V the device must function between 2.7 V and 3.3 V. This voltage range is often referred to as VDDmin and VDDmax. Functional tests must be executed over the entire range of the device specification, so the functional test vector sequence must be executed twice, once with VDD set to VDDmin and again set to VDDmax. Some device parameters (VIL/VIH/VOL/VOH) may be defined as a percentage of VDD. When this is the case be sure to adjust these parameters when modifying the value of VDD.

Gross Functional Tests

The term gross functional test refers to performing a functional test with relaxed conditions. Frequency, timings, voltages and current loading are generally relaxed. This test may also be called a basic functional test, loose test, or a wiggle test.

Why Perform a Gross Functional Test?

Performing a gross functional test indicates whether or not the device contains gross defects, in other words it ensures that the circuit is functionally “alive.” Test conditions should afford the best possible opportunity for the device to function correctly and pass the functional vector set. When the test program is initially being developed, the gross functional test conditions are often used to verify correct functionality of the entire vector set without regards to level and timing specifications. The gross functional test is often executed early in the test flow and is used to verify correct functionality of all test vectors that will be used throughout the entire test program when testing a new circuit design. Once the yield goals of the product are realized this test may be eliminated.



Relaxed Conditions
VIL = 0.0V VIH = VDD VOL/VOH = 1.5V

Figure 8-10 Gross Functional Testing

Figure 8-10 illustrates how the test conditions can be relaxed to test the 256 X 4 Static Ram. The test frequency, signal timings, and IO voltage levels have all been relaxed from their worst case values.

Gross Functional Test Method

Figure 8-10 on page 8-16 represents the gross functional timing for the 256 x 4 static RAM. The RAM AC specification shown in Chapter 9 states that the device operating frequency is 66 MHz. The gross functional test is performed with relaxed input levels, output levels, and timings. This example shows that the test frequency has been relaxed from 66 MHz to 1 MHz. All setup times, hold times, and propagation delays are also relaxed. It is necessary to maintain the same relative edge placements of all signals when relaxing the functional timings. This example also shows the relaxed values for VIL, VIH, VOL and VOH.

Once the device has passed the gross functional test, a more rigorous test may be executed to ensure that the device meets all of its specifications. As a means of increasing test throughput, the gross functional test may be executed conditionally only when a more rigorous test has failed. The gross functional test will often provide valuable yield information when used in production testing.

Gross Functional Test - Key Points:

- Purpose: to verify if the silicon is functional (alive)
- Functional test is executed with relaxed conditions
- Test conditions are not defined in device specifications
- Provides valuable yield information

Equation Based Timing

It is very important to develop the functional timing so that the timing values can be easily modified in the test program during development, debug, and characterization. The test timing may be developed as an equation using program variables. By simply modifying the value of the variable ***SCALE***., in this example, the entire program timing can be easily "tightened" or "relaxed". This technique can also be used to modify the timing between various tests, for example slow timing used within the gross functional test and fast timings used to verify the maximum operating speed of the device. When ***SCALE*** is set to 1, this example represents the timing for the 256 X 4 Static Ram as defined in the device AC Timing Specifications.

SCALE = 1;   /* Note: ***SCALE*** is a programmable variable that controls timing values */

```
WriteCycle       = 15E-9 * SCALE; /* 66MHz */
Address_edge1     =  0E-9;               Add_edge2     = 15E-9 * SCALE;
Data_In_edge1     =  2E-9 * SCALE;       Data_In_edge2 = 14E-9 * SCALE;
CS1_edge1         =  2E-9 * SCALE;       CS1_edge2     = 13E-9 * SCALE;
CS2_edge1         =  2E-9 * SCALE;       CS2_edge2     = 13E-9 * SCALE;
WE_edge1          =  2E-9 * SCALE;       WE_edge2      = 13E-9 * SCALE;
OE_edge1          =  2E-9 * SCALE;       OE_edge2      = 11E-9 * SCALE;
OUTPUT_VALID     = WriteCycle * 0.75;   STROBEWINDOW1 =  1E-9;
```

Figure 8-11 Equation Based Timing Example

Scalable timing- Key Points:

- Purpose: to ease the process of modifying related timings
- Can be developed as a relational timing diagram as defined in the device timing specification
- Can be used to generate timings for multiple speed devices

Functionally Testing a Device

The intent of the following discussion is to provide an overview of the relationship between the device specification, the test system hardware, and the test program for a basic functional test. A simple D Flip-Flop with Preset and Clear inputs is used to help explain this concept. This device features 4 inputs — CLK, D, PRE/ and CLR/; it also provides two outputs Q and Q/. The device functions as follows:

1. This is a positive-edge-triggered D-type flip-flop.
2. A low level on Preset (PRE/) or Clear (CLR/) sets or resets the outputs.
3. When PRE/ and CLR/ are inactive (high), data on the data input (D) meeting the setup and hold time requirements is transferred to the outputs on the positive-going edge of the clock.
4. The CLR/ input overrides the PRE/ input when both are low

Device Specification

The data below define the levels and timing needed to control the flip-flop. Specifications generally represent the worst case conditions that a device must meet. It is up to the test engineer to develop a plan for implementing these conditions on the test system. The flip-flop timing diagram Figure 8-12 illustrates one possible way this specification may be implemented on a test system.

The device specification states the following:

VCC = 1.8 V

VIH = VCC * .65 therefore VIH = 1.17V
VIL = VCC * .35 therefore VIL = 0.63 V

VOH = VCC * .67 therefore VOH = 1.2 V
VOL = VCC * .27 therefore VOL = 0.45 V

Operating frequency = 250 MHz
CLK minimum pulse duration = 1ns

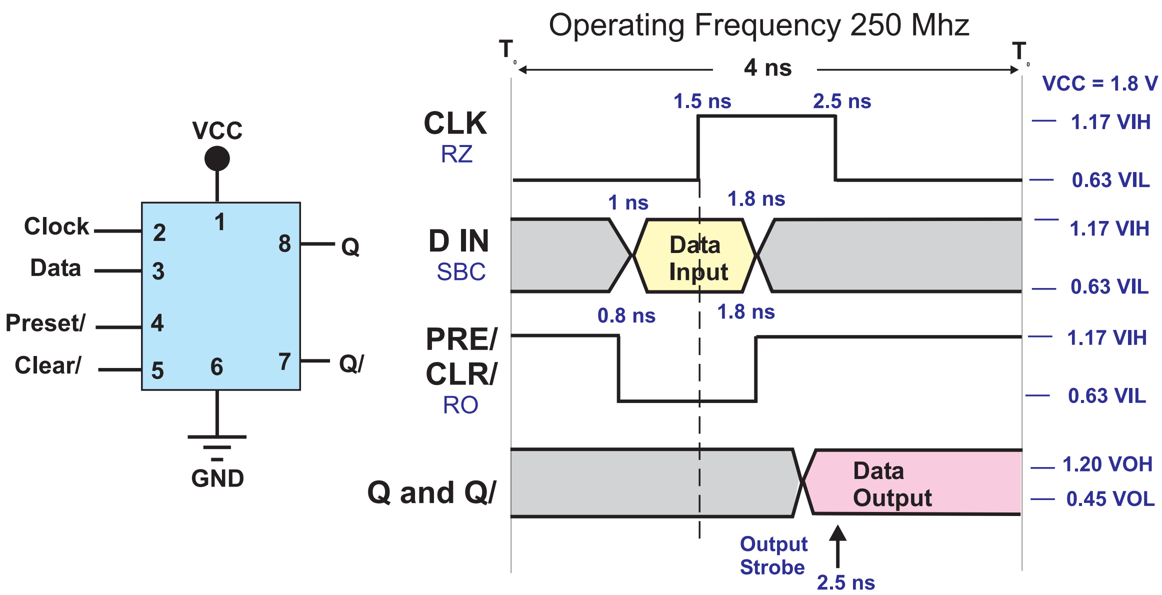
PRE/ minimum active pulse duration = 1ns
PRE/ minimum active after positive CLK = 0.3 ns (minimum time before inactive state)

CLR/ minimum active pulse duration = 1ns
CLR/ minimum active after positive CLK = 0.3 ns (minimum time before inactive state)

Data In Setup time = 0.5 ns (minimum time required before positive clock edge)
Data In Hold time = 0.3 ns (minimum time required after positive clock edge)

Propagation (Tpd) delay = 1 ns (maximum time from positive clock edge to data out)

Note: See Chapter 9 *"Testing AC Parameters"* for additional information regarding Setup time, Hold time, and Propagation delay measurements.



Cycle timing, signal formats, input edge timings and output strobe placement must be determined from the device specification

Figure 8-12 D Flip-Flop Test Conditions

The Items Needed to Test this Device

- Test hardware and fixtures — interface hardware, test socket, by-pass capacitors and wiring
- Device power, VCC, and Ground
- Input reference levels, VIL (logic 0,) and VIH (logic 1)
- Output reference levels, VOL (logic 0), and VOH (logic 1)
- Signal timing and format conditions for inputs and strobe timings for outputs
- A test vector pattern to verify logical functions

Programming Tester Resources

In order to guarantee that the device meets its specification the test hardware must be programmed in a manner that will verify each parameter. First, one of the test system DPS units (device power supplies) will be used to provide VCC. VCC will be set to1.8 V as defined in the device specification. Ground will be supplied by the ground plane of the test hardware.

The voltage references will provide the pin electronics driver circuitry with the correct input levels. VIL will be set to 0.63 V and VIH will be set to 1.17 V. The voltage references also supply the proper output reference levels. The outputs will be functionally tested with the comparator reference levels set to 0.45 V for VOL and 1.2 V for VOH.

The test system timing resources are used to define the test cycle time, the signal formats, and edge placements for the input signals and the time at which the output signals will be sampled. The first step in developing the timing is to determine the test cycle time. The device specification defines the test frequency as 250 MHz, this equates to a test cycle time of 4 ns by using the formula cycle_time = 1/frequency. The specification also states that the clock has a minimum pulse width of 1 ns. For this example the clock will be low for the first 1.5 ns of the cycle, high for 1 ns and low for the last 1.5 ns. In order to produce the correct signal format for CLK the RZ (return-to-zero) format will be used.

The PRE/ and CLR/ input timings are also referenced to the positive edge of the CLK signal. The specification states that the minimum pulse width is 1 ns and the active state of the signal must remain constant for a minimum of 0.3 ns after the positive CLK transition. Therefore the worst-case timing requires that these signal become active 0.7 ns before CLK and remain unchanged until 0.3 ns after. The PRE/ and CLR/ inputs are active low signals, these will require the use of RO (return-to-one) format.

The data input (D) timing is referenced to the CLK signal. The setup time specification states that the data signal must be valid 0.5 ns before the positive clock transition and must remain valid for the specified hold time of 0.3 ns after the positive transition, therefore the total pulse width of data will be 0.8 ns. In order to correctly verify the Setup and Hold time parameters the signal format must be SBC (surround-by-complement). Setup and Hold time parameter testing will be explained in detail in a later chapter.

The final step in developing the test timing is to establish the timing for the output pins. The device specification states that the output propagation delay is 1 ns, and is referenced to the positive edge of the CLK. The positive edge of CLK will occur at 1.5 ns so the outputs will need to be tested 1ns later. Outputs are verified by using a section of the test hardware known as the output strobe marker, so for this example the output strobe will be programmed to occur at 2.5 ns. If the outputs are in the correct logic state (as predicted by the truth table) at the time the output strobe occurs and if the outputs meet the correct voltage levels as set by the VOL and VOH references the functional test will result in a pass conditions. The output propagation delay parameter (Tpd) will be explained in detail in a later chapter.

A test pattern will be needed to verify correct functionally of the DUT. The test pattern can be hand written since the function of the sample device is simple. The test pattern will be stored in the test vector memory and executed each time the functional test is active.

The Test Vector Pattern

A test vector pattern, also called a truth table, must be created. The test vectors will be used during the functional test to verify that the DUT is capable of performing its logical functions correctly. Test vector patterns typically consist of a set of characters that represent logic states to be applied to the input pins and the expected response of the output pins. The sample test vector pattern for this device has eight vector states, each vector representing the data for a single cycle. Many possible vector sequences could be designed for this device, the eight vectors shown here are only one example, you may be able to think of additional states that would be useful for testing the logic of the flip-flop. The test vector data are combined with the timing, format, and level information to create the complete test as shown in Figure 8-13 on page 8-23. The test vectors for the D flip-flop are shown in Table 8-5 on page 8-22.

The characters used in the vector pattern represent:

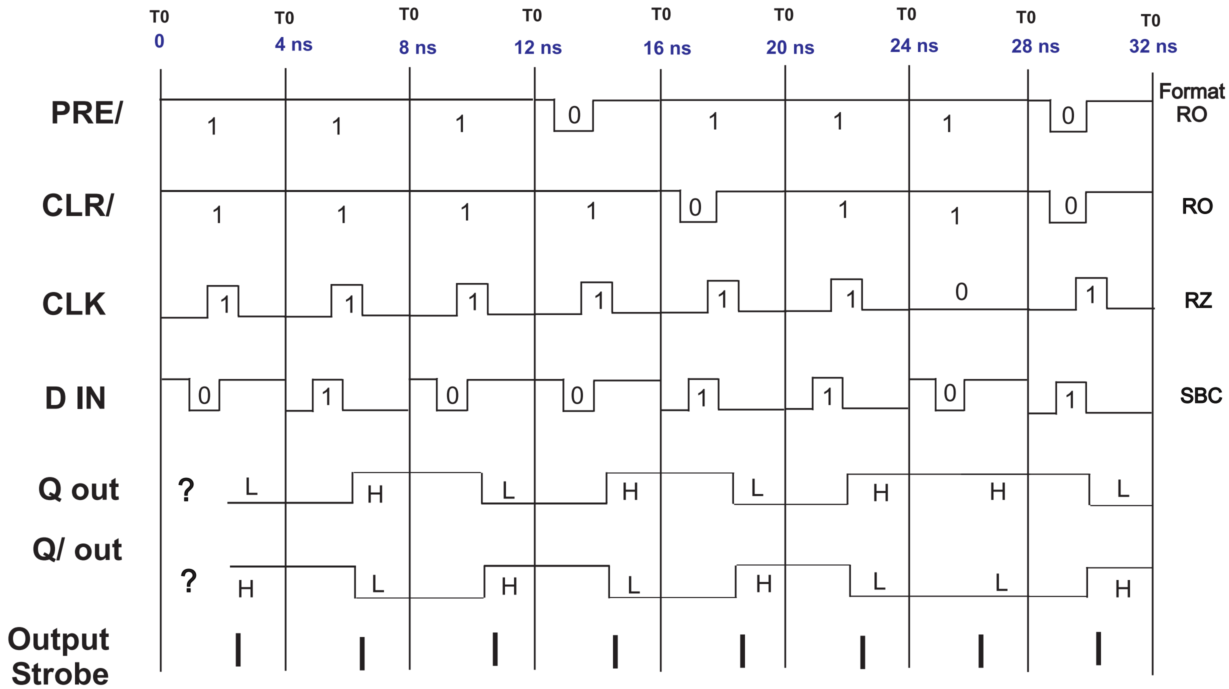
1 Drive input high (to logic 1)
0 Drive input low (to logic 0)
H Compare output to a high
L Compare output to a low

PRE/	CLR/	CLK	D	Q	Q/	REMARKS
1	1	1	0	L	H	Input 0 test
1	1	1	1	H	L	Input 1 - low to high transition Q out
1	1	1	0	L	H	Input 0 - high to low transition Q out
0	1	1	0	H	L	Preset Active - force Q to high
1	0	1	1	L	H	Clear Active - force Q to low
1	1	1	1	H	L	Input 1 - force Q state change
1	1	0	0	H	L	Change input - no Clock - hold output state
0	0	1	1	L	H	PRE/ CLR/ both active - Q forced low

Table 8-5 Test Vectors for the D Flip-Flop

Specification Test Conditions for the D Flip-Flop

Figure 8-13 shows the activity that will occur during the execution of the functional test. The timing diagram shows eight cycles of test vector data combined with the signal timings, signal formats and voltage levels. The information shown in this diagram reflects the conditions as defined in the device specification. The functional test rate is set to 4 ns, and CLK is in RZ signal format. The D input has the correct setup and hold timing and is in SBC signal format. PRE/ and CLR/ also have the correct setup and hold times and are in RO format. The format definitions will produce the proper wave shapes needed to verify the worst-case timings. The input and output levels are also set to the values defined in the device specification.



VCC 1.8, VIL .63, VIH 1.17, VOL .45, VOH 1.2

Figure 8-13 D Flip-Flop Timing for Specification Tests

Gross Functional Test Conditions for the D Flip-Flop

The purpose of the gross functional test is to determine if the device is functionally “alive” without regards to the exact values defined in the device specification. When all worse-case parametric specifications are applied to the device and the test fails, the failure may be caused by a sensitivity to one or more parameter values such as input levels, output levels, or timings. It may also fail because of physical defects in the silicon or due to an error during the fabrication processing. By executing a gross functional test you separate failures caused by parametric sensitivities from failures caused by non-functional silicon.

The waveform display shown in Figure 8-13 represents the timing and voltage conditions that would be used in a gross functional test. The input and output voltage levels have been modified (relaxed) in a manner that will make it easier for the device to function. When a parameter value is relaxed, its value is adjusted in a way that will make it easier for the DUT to function properly. For example, VIL can be relaxed by setting the value to 0.0 V. By lowering the value of VIL it becomes easier for the DUT to detect the input voltage as a logic 0. To relax inputs, lower the VIL levels and raise the VIH levels. VIH can be raised to VCC. To relax outputs, set both VOL and VOH to VCC/2, the comparators will then sense any output voltage below 0.9 V as a logic 0 and any voltage above 0.9 V as a logic 1.

In Figure 8-14 the timing has been relaxed by a factor of 10. To relax timing values, reduce the test rate, increase pulse widths, increase setup and hold times and increase output propagation delay limits. Notice that the test rate (cycle) has been reduced from 4 ns to 40 ns and all other timings have scaled with the test rate. The clock pulse width increased from 1 ns to 10 ns. The setup and hold times for D changed from 0.5 ns and 0.3 ns to 5 ns and 3 ns. The setup and hold times for PRE/ and CLR/ changed from 0.7 ns and 0.3 ns to 7 ns and 3 ns The output propagation delay timing has also been increased proportionately, from 1 ns to 10 ns, giving the output more time to change state and stabilize.

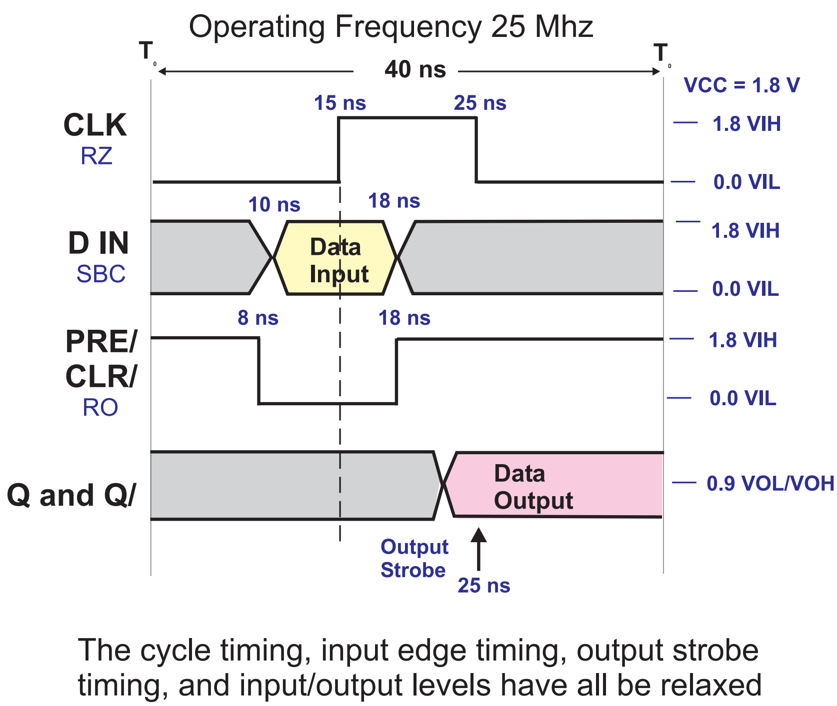
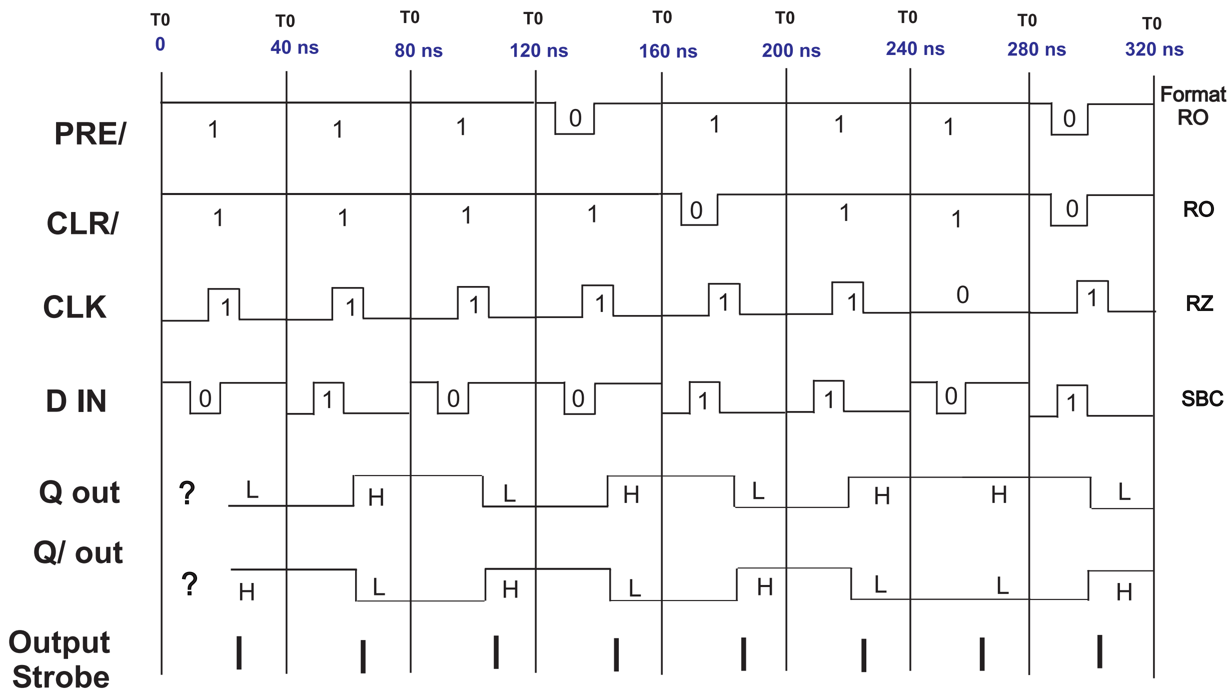


Figure 8-14 D Flip-Flop Gross Functional Test

If the device is tested to its specification, as in Figure 8-13 and fails, then retested and passes with relaxed conditions as in Figure 8-14, the failure was not caused by dead (totally non-functional) silicon. Each parameter can then be individually tested to specification to determine the actual sensitivity that caused the failure. Gross functional test conditions may be useful during the course of developing and verifying the test vector patterns.



VCC 1.8, VIL .0, VIH 1.8, VOL .9, VOH .9

Figure 8-15 D Flip-Flop Gross Functional Test Vector Sequence

Test Program Statements for the D Flip-Flop

A very basic functional test program is shown for the D flip-flop using a non-tester specific pseudo code. These statements setup the conditions based upon the device specification, and include Scalable Timing, but do not include conditions for the Gross Functional Test:

```
Begin Program;
/* Pin List */
VCC DPS1 pin 1;
CLK input pin 2;
D_in input pin 3;
PRE/ input pin 4;
CLR/ input pin 5;
GND pin 6; /* ground is hard wired */
Q/ output pin 7;
Q output pin 8;
/* Voltage Levels */
Force DPS1 1.8V;
Set VIL 0.63V; Set VIH 1.17V;
Set VOL 0.45V; Set VOH 1.2V;

/* Timings - SCALE can be modified to globally control the timing values. CLK
timing edges can be adjusted and all input and output timings will track auto-
matically */
```

```
SCALE = 1;
Cycle        = 4E-9 * SCALE; /* 250MHz */
CLK_edge1    = 1.5E-9 * SCALE;
CLK_edge2    = 2.5E-9 * SCALE;
D_in_edge1   = CLK_edge1 - (0.5E-9 * SCALE);
D_in_edge2   = CLK_edge1 + (0.3E-9 * SCALE);
PRE_edge1    = CLK_edge1 - (0.7E-9 * SCALE);
PRE_edge2    = CLK_edge1 + (0.3E-9 * SCALE);
CLR_edge1    = CLK_edge1 - (0.7E-9 * SCALE);
CLR_edge2    = CLK_edge1 + (0.3E-9 * SCALE);
TPD          = CLK_edge1 + (1.0E-9 * SCALE);

Set Test Period Cycle;
Set CLK tmarker1 CLK_edge1; Set CLK tmarker2 CLK_edge2;
Set CLK format RZ;

Set D_in tmarker1 D_in_edge1; Set D_in tmarker2 D_in_edge2;
Set D_in format SBC;

Set PRE/ tmarker1 PRE_edge1; Set PRE/ tmarker2 PRE_edge2;
Set PRE/ format RO;

Set CLR/ tmarker1 CLR_edge1; Set CLR/ tmarker2 CLR_edge2;
Set CLR/ format RO;

Set edge_strobe Q TPD; Set edge_strobe Q/ TPD;

/* load the vectors into vector memory */
Load Test_pattern (flip_flop_test_vectors);

/* Run the test */
Burst Test_pattern;

/* Turn off voltage levels */
Set VOL 0.0V; Set VOH 0.0V;
Set VIL 0.0V; Set VIH 0.0V;
Force DPS1 0.0V;

End Program;
```

STIL Statements for the D Flip-Flop

A similar program can be created using STIL (Standard Tester Interface Language) IEEE-1450 statements. The following code illustrates the program in STIL format. The timing is defined as per the device specification and is not scalable.

```
STIL 1.0 {Design 2006; DCLevels 2006;}
Signals {
    Data In;
    Clk In;
    Pre_ In;
    Clr_ In;
```

```
    QD Out;
    QB Out;
}

SignalGroups {
    PreClr = 'Pre_ + Clr_';
    QQB    = 'QD + QB';
    All_In = 'Pre_ + Clr_ + Clk + Data';
    All    = 'All_In + QQB';
}

DCLevels DC_Spec {
    All {
        VIL 0.63V;
        VIH 1.17V;
        VOL 0.45V;
        VOH 1.2V;
    }
}

DCLevels DC_Powerdown {
    All {
        VOL 0.0;
        VOH 0.0;
        VIL 0.0;
        VIH 0.0:
    }
}

Timing Time_Spec{
    Waveformtable Basic {
        Period 4ns;
        Waveforms {
            Clk {
                01 {0ns D; 1.5ns D/U; 2.5ns D;}
                }
            PreClr {
                01 {0.8ns D/U; 1.8ns U;}
                   }
            Data {
                01 {0ns U/D; 1ns D/U; 1.8ns U/D;}
                 }
            QQB  {
                HLX {2.5ns H/L/X;}
                 }
    }
}

PatternBurst FF_vectors {
    PatList {Flip_Flop_test_vectors}
}
```

```
PatternExec FF_Spec {
    PatternBurst FF_vectors;
    DCLevels DC_Spec;
    Timing Time_Spec;
    DCLevels DC_Powerdown;
}
```

Note: STIL vectors are shown below.

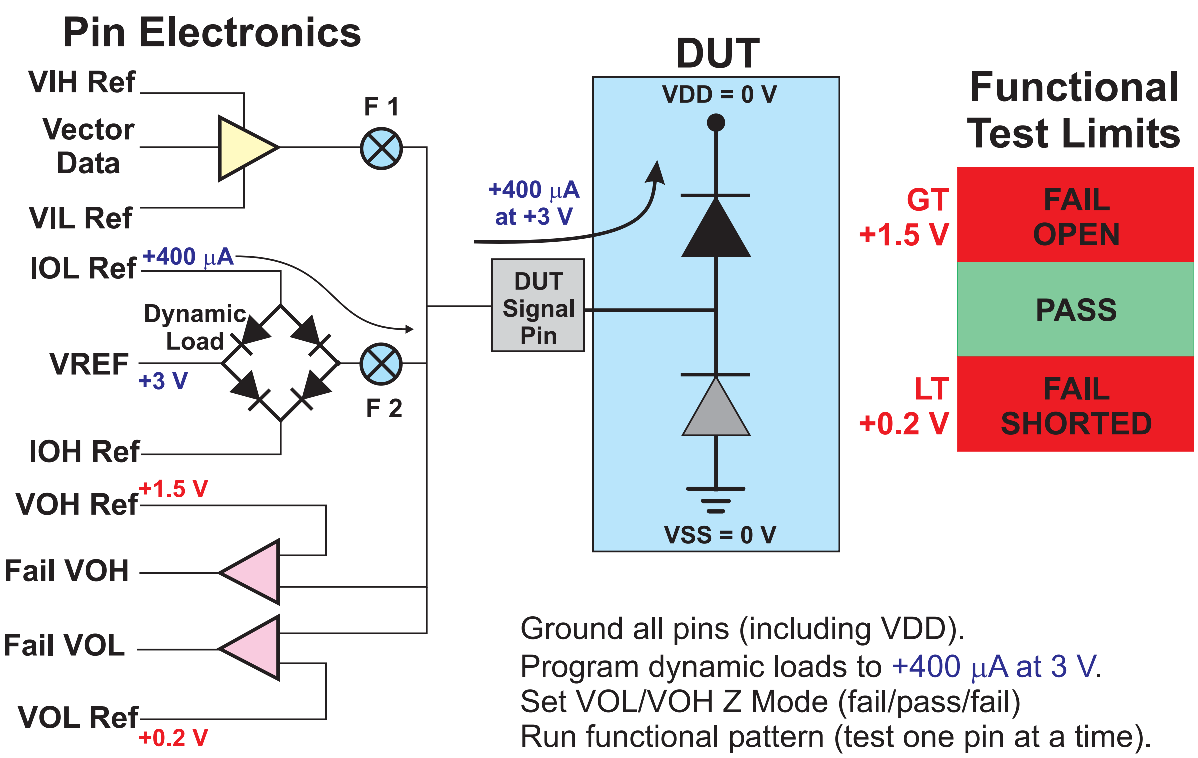
```
Pattern Flip_Flop_test_vectors {
W Basic;
V {All=1110LH;}
V {All=1111HL;}
V {All=1110LH;}
V {All=0110HL;}
V {All=1011LH;}
V {All=1111HL;}
V {All=1100HL;}
V {All=0011LH;}
}
```

Standard Functional Tests

Although each unique circuit design requires an individual set of functional test conditions, there are a few parameters that may be verified functionally using standard test methodologies. Let's look at a few of these parameters, keeping in mind that what is being explained is a standard methodology to functionally verifying the given parameter. You will notice that some of these tests have previously been discussed using DC test methodologies.

Opens and Shorts - Functional Method

A faster and less costly way to test for opens and shorts is to do it as a functional test rather than as a DC test. First, the functional test timing must be defined. For this example a 1µs test period is used. Each pin is functionally tested, so output strobe timing must be set. The strobe placement is set to occur at 900ns and to have a 1ns width. See Figure 8-17 on page 8-31 for a functional timing diagram.



Ground all pins (including VDD).
Program dynamic loads to +400 µA at 3 V.
Set VOL/VOH Z Mode (fail/pass/fail)
Run functional pattern (test one pin at a time).
Test for diode voltage.
Fails if Voltage is greater than 1.5 V.
Fails if Voltage is less than 0.2 V.

Figure 8-16 Opens and Shorts Test

All signal pins must be tied to ground. This is done by defining all signal pins as inputs and applying VIL (set to 0 V) through the pin electronics. All power pins, VDD and VSS, must be connected to ground (0 V). The dynamic current loads supply the current and voltage needed to forward bias the VDD protection diode. The programmable loads supply 400 µA of current. The load reference voltage (Vref) is set to +3 V. The output comparator levels must be programmed so that a center pass region is defined (often called “setting the comparators to mid–band or Z-state mode”). The VOL level is set to +0.2 V and the VOH level is set to +1.5 V. See Figure 8-17 on page 8-31.

A functional test pattern must be developed which will execute the following sequence:

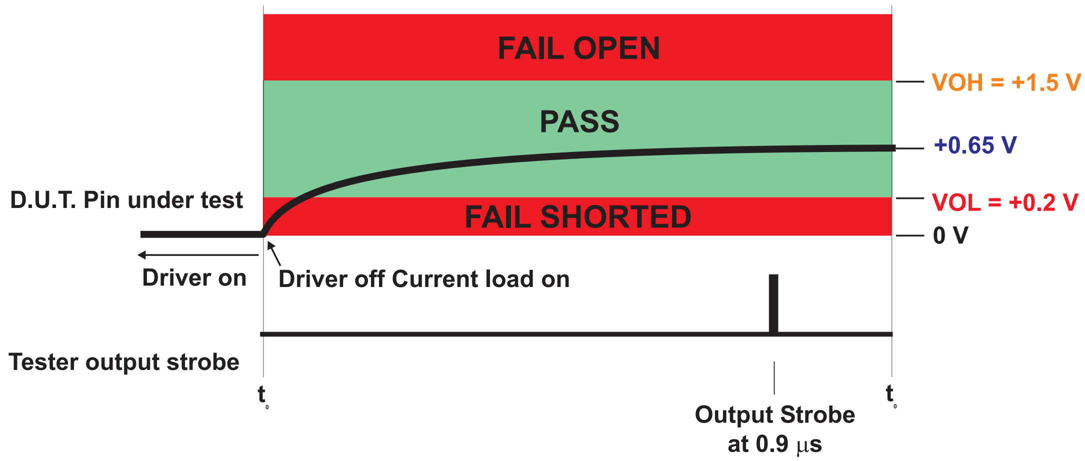
Cycle	Action
1	Define all signal pins as inputs and force VIL (0 V). The character “0” in the vector file instructs the tester to perform this function on each pin.
2	Define the first signal pin as an output to be tested, turn off the tester drive on that pin, and compare output for pass/fail. The “Z” character instructs the tester to perform this function on the single pin to be tested.
3	Turn the driver back on for the pin tested in the last cycle and repeat step two for the next pin to be tested.
4	Repeat steps 2 and 3 until all signal pins are tested through cycle 6.

Sample Test Vector File for Opens/Shorts

```
00000               /* cycle 1 ground all pins */
Z0000               /* cycle 2 test for diode on first pin */
0Z000               /* cycle 3 test for diode on second pin */
00Z00               /* cycle 4 test for diode on third pin */
000Z0               /* cycle 5 test for diode on fourth pin */
0000Z               /* cycle 6 test for diode on fifth pin */
                    /* the next cycle is executed separately */
ZZZZZ               /* cycle 7 turns the drivers off and tests all pins */
```

When the walking Z test pattern is executed, the first signal pin is tested in cycle 2. Once the tester pin driver is shut off the dynamic current load begins to pull the device pin toward +3 V, which is supplied by Vref. If a working diode exists it will turn on when the voltage reaches +0.65 V. The diode will then clamp the Vref voltage at that point, while sinking the +400 µA supplied by the IOL side of the programmable current load.

When the pass/fail comparison is made, the test will pass because the tester comparators will sense the +0.65 V which is within the upper VOH limit of +1.5 V and also within the lower VOL limit of +0.2 V. If a short occurs, the comparators will sense 0 V; if an open occurs the comparators will sense +3.0 V. Either case will result in a failure.



Pin driver forces 0V in prior cycle.
Pin driver turns off, current load turns on at start of period.
Output strobe allows time for pin voltage to settle.
If pin is good, output charges to 1 diode voltage (+0.65 V).
If pin is open, output charges to VREF (GT +1.5 V).
If pin is shorted, output stays low (LT +0.2 V).

Figure 8-17 Opens and Shorts Timing - Functional Method

The timing diagram indicates a test period of 1µs (1 MHz). At the start of the cycle the driver turns off for the pin under test and the current load turns on. The current load will pull the pin under test towards the Vref voltage. If there is a working diode with no shorts the comparators will sense a valid diode drop and the test will pass. Notice the output strobe is placed at 900 ns into the cycle, this allows sufficient time for the current load to stabilize and the diode to turn on, ensuring a solid test result.

Note: the purpose of the walking Z pattern, while testing the VDD diodes, ensures that no pin-to-pin shorts exist. If the pin under test is shorted to another device pin, it will show up as a failure since the pin it is shorted to is tied to ground.

Once all of the VDD diodes are tested for both opens and shorts, the lower VSS diodes must be tested. If all of the VDD diodes pass the test, there are no shorts on any device pin, otherwise the test would fail. The lower VSS diodes only need to be tested to ensure that they are not open. This can be accomplish by setting the conditions shown in Figure 8-18 on page 8-32 and then executing only test cycle 7, containing ZZZZ. All VSS diodes will be tested in parallel, in one single cycle, this will verify that no diodes are open.

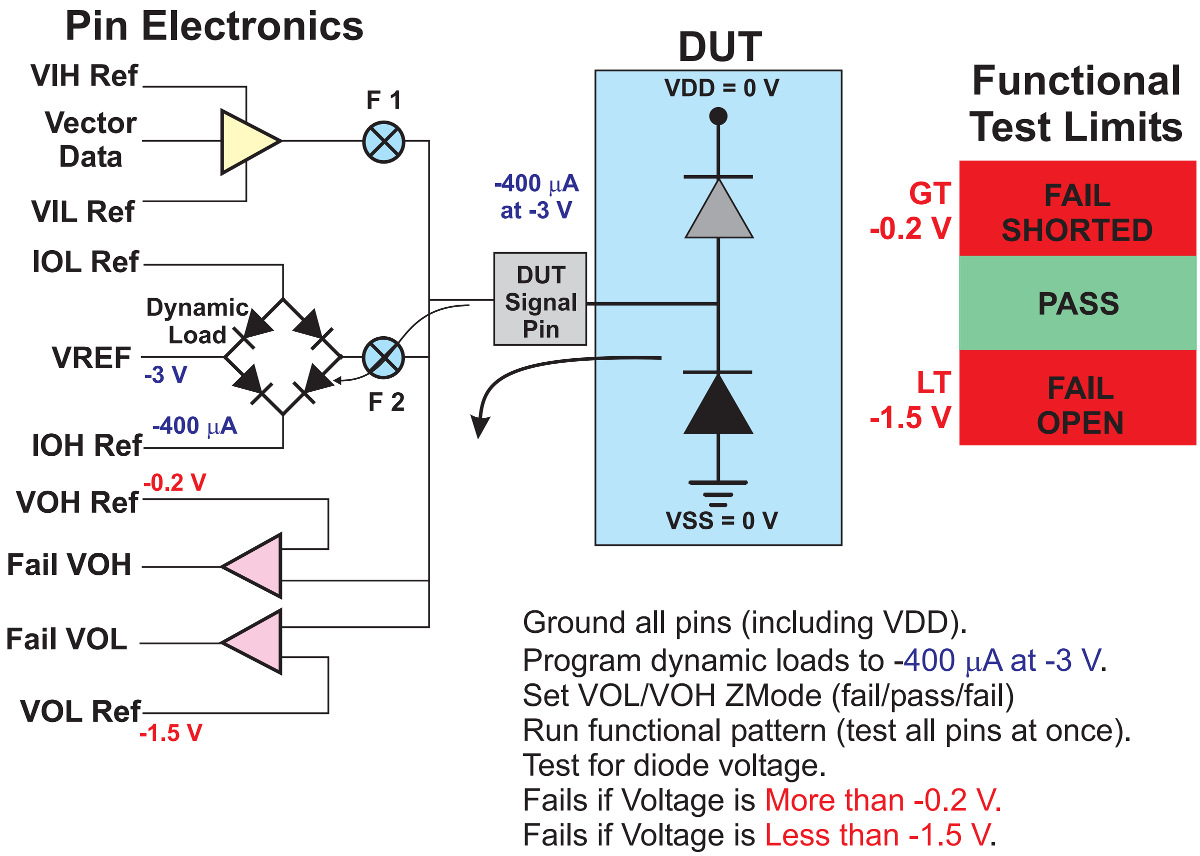


Figure 8-18 Opens and Shorts Timing - VSS Diode

The advantage of the Functional Opens/Shorts test is speed. The test will execute very fast compared to the DC serial/static method. The disadvantage is that the datalog results are somewhat harder to understand. Often, test operators are accustomed to seeing the DC readings produced by the serial/static method. By executing the serial/static test only when the Functional Opens/Shorts test fails, any DC readings on failed pins can be datalogged for operators without much additional test time.

Functional Shorts Datalog

The datalog shown in Figure 8-19 shows failures that occurred during the Functional Shorts test. The “+” character indicates the failing pins.

```
Test 1:     4:Stage 9, SHORTS:Shorts

S:Pattern                                   Start-Loc  Stop-Loc        Size  Mode

contact                                            3        103         101  norm

Result *FAIL*
------------------------------------------------------------------------

S          CRCEIITTTTIIIISDDIPPPPIPPPIIIIREIEEDOIOIDSSIODDTDDDDDDDDDDD
i          KSKXNNCMDDOOOOAOICISSSAOIOOOOOWRORRSCCLLOAYBBIORBBBBBBBBBBB
t          ITOMTTKSIOBBBBDE2KBEEECBDDBBBBNA AOEKKDDEDNFE1UA11111100000
e           B  10    IIIIDN_2FLLLKESSIIII M MML1111NDC11 TP54321098765
#                    TTTT22P__210 ___TTTT L H      111   1
                     3210__BPI___ OIO4567 O I
                     ____PP0BBODS BLL____
                     PPPPBB10FCOY EDDVVVV
1:       2 +0000000000000000000000000000000000000000000000000000000000
1:       6 0000+000000000000000000000000000000000000000000000000000000
1:      31 00000000000000000000000000000+00000000000000000000000000000
1:      37 00000000000000000000000000000000000+00000000000000000000000
1:      44 000000000000000000000000000000000000000000+0000000000000000
1:      55 00000000000000000000000000000000000000000000000000000+00000
1:      56 000000000000000000000000000000000000000000000000000000+0000
1:      57 00000000000000000000000000000000000000000000000000000000+00
```

Figure 8-19 Shorts Test Sample Datalog

Key Points

- Purpose: to detect open or shorted device pins and verify proper connections between the test system and the DUT.
- Functional Test serial/dynamic test method
- Uses programmable current loads and functional comparators
- Test requirements not found in device specifications
- Much faster than the DC serial/static method

VIL/VIH

VIL (Voltage Input Low) represents the worst-case voltage applied to an input to represent a logic 0. VIH (Voltage Input High) represents the worst-case voltage applied to an input to represent a logic 1. Table 8-6 shows the VIL/VIH specifications for the 256 x 4 Static RAM. The values indicated are typical for 3.3 V and 5.0 V logic.

Parameter	Description	Test Conditions	Min	Max	Units
VIH	Input HIGH Voltage		2.0	VDD	V
VIL	Input LOW Voltage		0.0	0.8	V

Table 8-6 VIH/VIL Sample Specification

Why Test for VIL/VIH?

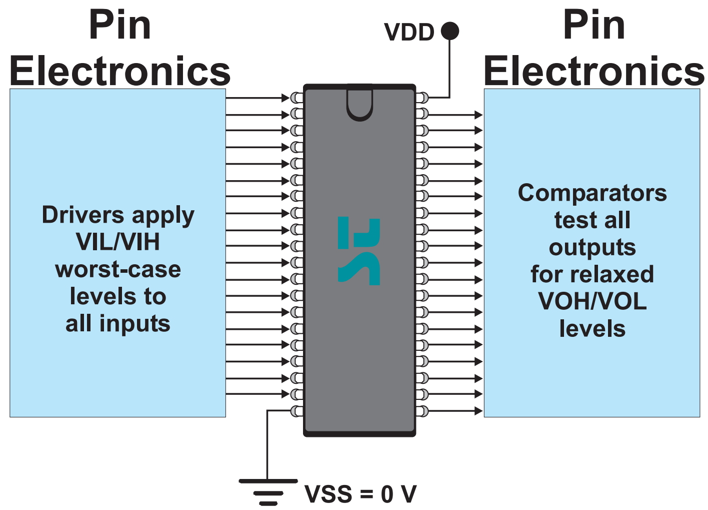
The VIL/VIH test guarantees that the input pins can correctly sense the proper logic states when the VIL/VIH voltages are applied. VIL represents the maximum voltage that the DUT is guaranteed to sense as a logic 0. VIH represents the minimum voltage that the DUT is guaranteed to sense as a logic 1.

VIL/VIH Functional Test Method

Although the VIL and VIH levels are often defined in the device specification under the heading “DC Characteristics”, they must be verified by performing a functional test. The test is performed by applying the input levels defined in the device specification and then executing a functional test pattern. If the test results in a pass, the device has operated correctly and meets the VIL/VIH specifications. If the test results in a fail, the device has not met the intended specification.

If the device design incorporates the IEEE 1194.1 Boundary Scan interface, observation of the input buffer performance is simplified. The Boundary Scan standard incorporates Boundary Scan Cells (BSC) that provides direct observation of the input buffers. The VIL/VIH specification levels are applied to the device input pins, the input buffer states are then clocked into the BSCs, and the results are shifted out of the Boundary Scan chain for observation. This eliminates the need to propagate the input data through the core logic and observe the results on the primary outputs of the device. It also provides a direct means of trouble-shooting and identifying problems.

Note: VIL/VIH requires 2 test iterations, one at VDDmin and one at VDDmax



Apply VDDmax.
Apply input levels as defined in specification.
Relax all other parameters and execute
functional test pattern.
Monitor output signals during test.
Fails test if any output level is different
from expected.
Repeat test at VDDmin.

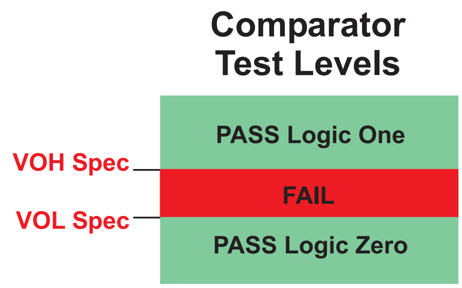


Figure 8-20 VIL/VIH Levels Test

VIL/VIH — Trouble Shooting

To begin trouble shooting, without the add of the Boundary Scan circuity, enable the datalogger and observe the test results. If a DUT standard (a known good device) is available, test it and observe the result.

When the VIL/VIH test fails, the failure appears as one or more incorrect output signals. When testing a complex device it is often difficult or impossible to determine which input is causing the failure unless each input is tested individually.

Start by relaxing both the VIL and VIH levels. Relax the VIL level by lowering it — 0 V is the most relaxed VIL voltage level. Relax the VIH level by raising it — VDD is the most relaxed VIH voltage level. After relaxing the input levels rerun the test. It should pass with the relaxed conditions. If it does not pass the failure is not caused by the VIL/VIH levels, you will need to look elsewhere for the cause of the failure.

Next set VIH back to the original specification voltage value and rerun the test. If the test passes then VIH meets the specification and the VIL parameter must be the cause of the failure. If the test fails, relax the VIH value on all but one pin and rerun the test. This will verify one pin at a time for VIH; this process can be repeated to verify VIL. Output current loading and high frequency testing can cause noise within the DUT that can affect the VIL/VIH test. It may be necessary to eliminate all output loading and to reduce the test frequency (increase the test period). The test system software may provide a “margins tool”, if so it can be used to quickly identify the threshold switching points of each input.

Read the device specification carefully — it may state that the VIL and VIH levels are valid only in a “static noise free environment.” This is an indication that the VIL and VIH levels may need to be relaxed somewhat when used in production testing.

VIL/VIH - Key Points

- Purpose: to verify that the input buffers will properly detect VIL and VIH voltage levels
- VIL/VIH can only be verified by executing a dynamic functional test
- Test limits are defined in device specifications (often as DC)
- Output pins fail as a result of improper operation of input circuitry

VOL/IOL VOH/IOH Functional Test

VOL (Voltage Output Low) represents the maximum voltage produced by an output when the output is in the low state. IOL (current (I) Output Low) represents the current sinking capabilities of an output when the output is in the low state. VOH (Voltage Output High) represents the minimum voltage produced by an output when the output is in the high state. IOH (current (I) Output High) represents the current sourcing capabilities of an output when the output is in the high state. The table below shows the VOL/VOH specifications for the 256 x 4 Static RAM.

Parameter	Description	Test Conditions	Min	Max	Units
VOH	Output HIGH Voltage	VDD = Min. IOH = -5.2mA	**2.4**		**V**
VOL	Output LOW Voltage	VDD = Min. IOL = 8.0mA		**0.4**	**V**

Table 8-7 VOL/VOH Sample Specification

Why Test Functionally for VOL/IOL VOH/IOH?

The VOL/IOL/VOH/IOH test verifies the resistance of output pins while driving valid output levels under a current load. This test ensures that the outputs will provide the specified IOL/IOH current while maintaining the correct VOL/VOH voltages. Performing the VOL/IOL/VOH/IOH test functionally has a significant speed advantage when compared to performing the same test using the serial/static PMU method.

VOL/IOL VOH/IOH — Dynamic Test Method

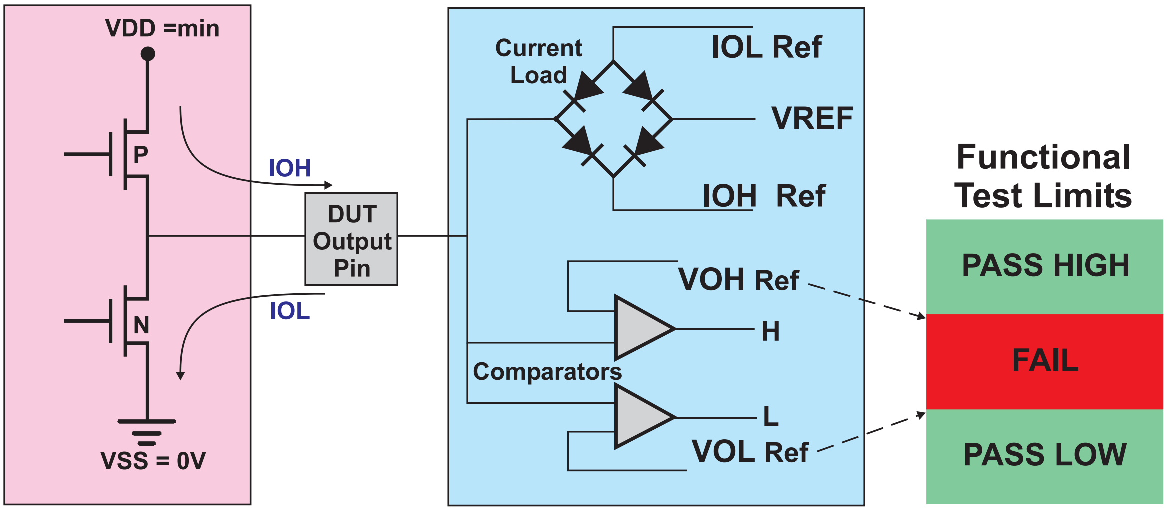
These parameters may be verified either statically or dynamically. To perform the test dynamically, the tester comparator levels are set to the specified VOL/VOH values, load currents are applied (programmable load or resistive load) and the functional test is executed.

During functional test execution, the outputs must sink and source the proper IOL/IOH currents and the functional output comparator circuitry ensures that the outputs maintain the proper VOL/VOH voltage. If an output is weak and cannot sink or source the proper current, then the comparators will detect a voltage that is outside of the VOL/VOH limits and the test will fail.

Loading the outputs during the execution of a functional test can result in high current within the DUT. If the DUT has a large number of outputs or it has high current output buffers, then it may not be possible to load all of the outputs at the same time and still meet the VOL/VOH voltage specification. High currents within the DUT may generate noise which can appear on the outputs and cause the comparators to fail the VOL/VOH levels. If this problem occurs apply loads to a small number of pins and execute the functional test. Repeat until all outputs have been properly loaded and tested. In some cases it may be necessary to decrease the test rate and move the output strobe time further into the cycle to achieve stable test results.

If the device design incorporates the IEEE 1194.1 Boundary Scan standard, control of the output buffers is simplified. The Boundary Scan standard incorporates Boundary Scan Cells (BSC) that provides direct control of the output buffer circuits. All ones are loaded into the BSC's and then transferred to the output buffers, driving the outputs high. The test system is then used to verify the VOH levels while suppling IOH current. This is repeated for the logic low state. Boundary Scan eliminates the need to control the output buffers via the core logic. It also simplifies trouble-shooting.

Be sure to check the specification for the exact voltage and current values to be used in the test program.



Set programmable loads to IOL/IOH spec for each output.
Set comparator levels to VOL/VOH spec for each output.
Execute the functional test pattern that tests all outputs for logic 0 and logic 1 levels.

Note: You may need to run the vector pattern at a reduced rate.

Figure 8-21 VOH/VOL Functional Test

VOL/IOL VOH/IOH - Trouble Shooting

To begin trouble shooting, enable the datalogger and observe the test results. If a DUT standard is available, test it and observe the result.

When the VOL/IOL VOH/IOH test fails, the failure appears as one or more incorrect output signals. The datalogger indicates which device pins failed and the failing states. Observe the failing results and see if failures are both ones and zeros. If so, both VOL and VOH levels are defective; if not, then only one parameter is causing the failure. Verify that the test can be made to pass by relaxing the VOL/VOH levels. The IOL/IOH currents can also be relaxed to try to make the test pass.

Note: The outputs will require more time to transition between logic levels when fully loaded with current, so it may be necessary to reduce the test frequency and move the output strobe timing to a later time in the test cycle to get the test to pass.

Functional VOL/VOH Datalog

The datalog in Figure 8-22 shows failures that occurred during the Functional VOL/VOH test. The “.”character indicates an output failing a zero (L) state, the “\” character indicates an output failing a one (H) state. The functional datalog makes it easy to see whether the device is failing a one level or a zero level, the failing signal is also indicated.

Functional Datalog for VOL/VOH Test

\ failed below VOH . failed above VOL

\ expected H . expected L

```
Test 14:    VOLVOH
BSCAN:Pattern           Start-Loc  Stop-Loc        Size  Mode
                            13188     14621        1434  norm
Result *FAIL*
-----------------------------------------------------------------------

S         CRCEIITTTTTIIIISDDIPPPPIPPPIIIIREIEEDOIOIDSSIODDTDDDDDDDDDDD
i         KSKXNNCMDDOOOOAOICISSSAOIOOOOOWRORRSCCLLOAYBBIORBBBBBBBBBBB
t         ITOMTTKSIOBBBBDE2KBEEECBDDBBBBNA AOEKKDDEDNFE1UA11111100000
e          B  10    IIIIDN_2FLLLKESSIIII M MML1111NDC11 TP54321098765
#                   TTTT22P__210 ___TTTT L H      111   1
                    3210__BPI___ OIO4567 O I
                    ____PP0BBODS BLL____
                    PPPPBB10FCOY EDDVVVV
1:   13285 10XX01ZZ.\0LLZZZZZZZZZ010100HHLHXX010LHL01XXX010LLLLH\XLLLL
1:   13978 10XX01ZZ.\0LLZZZZZZZZZ010100HHLHXX010LHL01XXX010LLLLHHXLHLL
1:   13986 XX01ZZLH0LLZZZZZZZZZ010100HH.HXX010LHL01XXX010LLLLHHXLLLL10
```

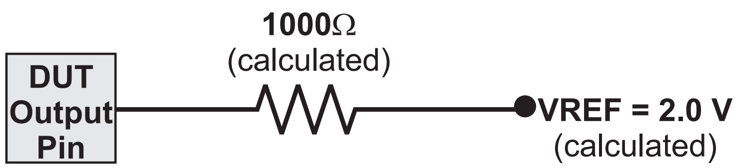
Figure 8-22 VOH/VOL Test Sample Datalog

VOL/IOL VOH/IOH - Key Points

- Purpose: to verify that the output buffers will properly supply the correct amount of current (IOL/IOH) at the proper voltage (VOL/VOH)
- Dynamic functional test must be executed
- Test limits defined in device specifications
- Test requires current loads on output pins
- It may not be possible to test all output pins simultaneously when fully loaded due to noise produced by high currents

Resistive Output Loading

When using a test system that does not offer programmable current loads, resistive loads can be added to the external test hardware to supply the IOL/IOH currents. Figure 8-23 is an example of a single resistive load. The device specification defines the values of VOL/IOL and VOH/IOH. The following formula calculates the reference voltage (Vref) and a single resistor value required to satisfy the specification.



Specification	Ohm's Law
VOL = 0.4 V	E = IR
VOH = 2.4 V	I = E/R
IOL = 1.6 mA	R = E/I
IOH = 400 µA	

Figure 8-23 Output Loading

To calculate the reference voltage:

```
Vref = ((IOL * VOH) + (IOH * VOL)) / (IOL + IOH)
```

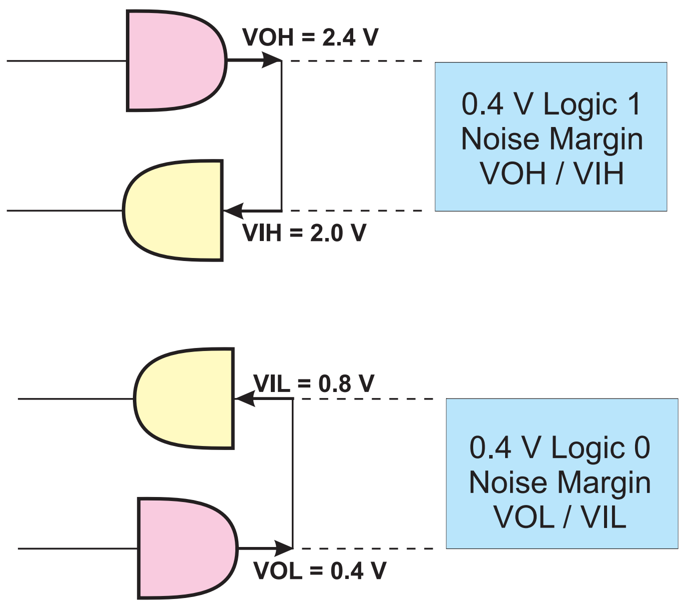
To calculate the resistance value:

```
Resistor = (Vref - VOL) / IOL
```

Input/Output Levels Relationship

Figure 8-24 shows the relationship between VIL/VIH levels and VOL/VOH levels. For 3.3 V and 5.0 V logic, input levels are typically specified as 0.8 V and 2.0 V and output levels as 0.4 V and 2.4 V. In the use of semiconductors, the output of one device is most often connected to the input of another device.

When testing to the above specifications, it can be seen that a 400 mV noise margin exists between input and output levels. VOH is guaranteed to be 2.4 V or greater, and the input level VIH is guaranteed to detect 2.0 V or greater as a logic 1. The same applies to VOL and VIL — VOL is guaranteed by testing to provide a voltage which is 400 mV lower than the specified value of VIL.



Testing Input VIL/VIH and Output VOL/VOH levels guarantees a level of Noise Margin

Figure 8-24 Input/Output Levels

Functional Z State / High Impedance Testing

When a device has bidirectional pins or three state outputs, there can be many logic conditions under which the output buffers must be in its high impedance state. These conditions depend on the functional test pattern sequences, and outputs must be checked for the correct high impedance state under all of these conditions, thus the Z–State test.

Why Test Z–State Functionally?

The functional Z–State test (also Tri-State or three state) verifies that the DUT outputs can achieve the proper high impedance state while the device is actively executing vector patterns.

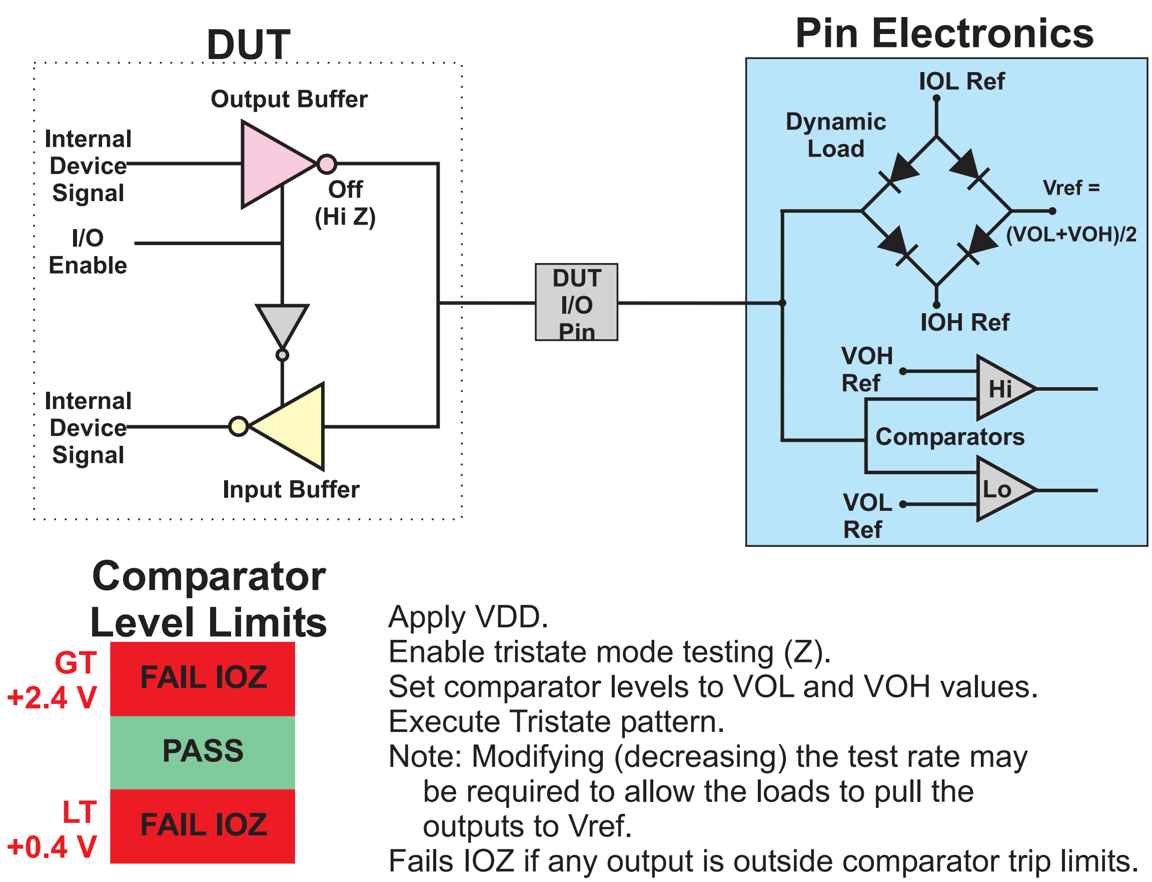


Figure 8-25 Functional Z-State Test

Functional Z–State — Test Method

The Z–State high impedance (Tri–State) test is made to ensure that bi–directional and high impedance outputs are capable of achieving a high impedance or off state. Some test systems have the ability to perform this test functionally. When performed as a functional test, Tri–State output conditions are tested dynamically.

Functional Tri–State testing requires programmable loads or external resistive loads. The reference voltage (Vref) of the load must be programmed to a value between the VOH and the VOL compare level. Often, (VOL+VOH)/2 is used. As the output under test enters a high impedance state, it loses the ability to sink or source current. The test load then pulls the output to the intermediate value (not H and not L). The comparators are set to tri–state mode testing. This provides a pass zone, surrounded above by a fail zone (logic H) and below by a fail zone (logic L). Review Figure 8-25 on page 8-42 for more on high impedance level testing.

The exact conditions for functional high impedance testing are not normally defined in the device specification, so some experimentation may be required to produce a reliable test. When the output of the DUT enters a high impedance state it becomes the responsibility of the test system to provide the intermediate voltage level. The amount of time required for the intermediate level to be reached depends on how much current the output load delivers and on the capacitive loading of the tester channel. This test can be sensitive to changes in test hardware — different results may be experienced between wafer test, hand test and auto handler test due to the different capacitive loads presented.

Functional Tri-state Datalog

The datalog in Figure 8-26 shows failures that occurred during the Functional Tri-State test. The "**v**" character indicates an output that failed the Tri-State level because it was below the VOL reference voltage. The "**^**" character indicates an output that failed the Tri-State level because it was above the VOH reference voltage. The functional datalog makes it easy to see which signal is failing.

Functional Datalog of Tristate Test

```
                    ^ failed above VOH   v failed below VOL

     Note: this test system datalog indicates failure as above/below Z-state

Z:Pattern                      Start-Loc  Stop-Loc        Size  Mode
TriState:Pattern                     104     57180       57077  norm
Result *FAIL*
---------------------------------------------------------------------
S         CRCEIITTTTIIIISDDIPPPPIPPPIIIIREIEEDOIOIDSSIODDTDDDDDDDDDD
i         KSKXNNCMDDOOOOAOICISSSAOIOOOOOWRORRSCCLLOAYBBIORBBBBBBBBBB
t         ITOMTTKSIOBBBBDE2KBEEECBDDBBBBNA AOEKKDDEDNFE1UA1111100000
e          B  10     IIIIDN_2FLLLKESSIIII M MML1111NDC11 TP54321098765
#                    TTTT22P__210 ___TTTT L H       111   1
                     3210__BPI___ OIO4567 O I
                     ____PP0BBODS BLL____
                     PPPPBB10FCOY EDDVVVV
1:      1 XXXXXXXXXXZZZXXXXXXXXXXXXXZZZZXXXvXXXXXXXXXXXXXXXXZZZZZZZZZ
1:     48 XXXXXXXXXXvvvZXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
1:     49 XXXXXXXXXXZvvZXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
1:     50 XXXXXXXXXXZvZZXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
1:     51 XXXXXXXXXXZZZXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX^ZZZZZZZZ
1:     70 XXXXXXXXXXvvvZXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
1:     71 XXXXXXXXXXZvvZXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
```

Figure 8-26 Functional Z-State Test Sample Datalog

Functional Z–State — Trouble Shooting

To begin trouble shooting, enable the datalogger and observe the test results. If a DUT standard is available, test it and observe the result.

When the Functional Z–State test fails, the failure appears as one or more incorrect output signals. The datalogger will indicate which device pin(s) failed. If the test vector pattern is testing only for high impedance output states, remove the device from the test socket and repeat the test. An open socket will pass the test. If the test vector pattern is testing for both high impedance states and valid logic states an open socket test will fail the valid logic states.

This test is affected by the VOL/VOH comparator levels, the IOL/IOH currents that are supplied by the current loads and by the Vref voltage supplied by the current loads.

Additional time may be required to transition from a valid logic level to the tri–state level, so it may be necessary to slow down the test frequency and move the output strobe timing to a later point within the test cycle in order to get the test to pass.

Functional Z–State — Key Points

- Purpose: to ensure that bi–directional and high impedance outputs can achieve a high impedance or off state
- Dynamic functional test must be executed
- Test conditions are not defined in device specifications
- Test requires loads on outputs to provide intermediate voltage
- Test is affected by external capacitance on outputs

Open Drain / Open Source Outputs

The device specification will indicate if any output pins have open drain or open source outputs. Be sure to note this when reviewing the device specification because these outputs will require special considerations. Open drain outputs can only drive low — they only sink current. They cannot drive high because there is no pull–up circuitry in the DUT. The output signal must be pulled high by some external means such as a resistor or current load.

Open source outputs are just the opposite. They can drive high, but not low — they can only source current because there is no pull–down circuitry in the DUT. The output signal must be pulled down by some external means such as a resistor or current load.

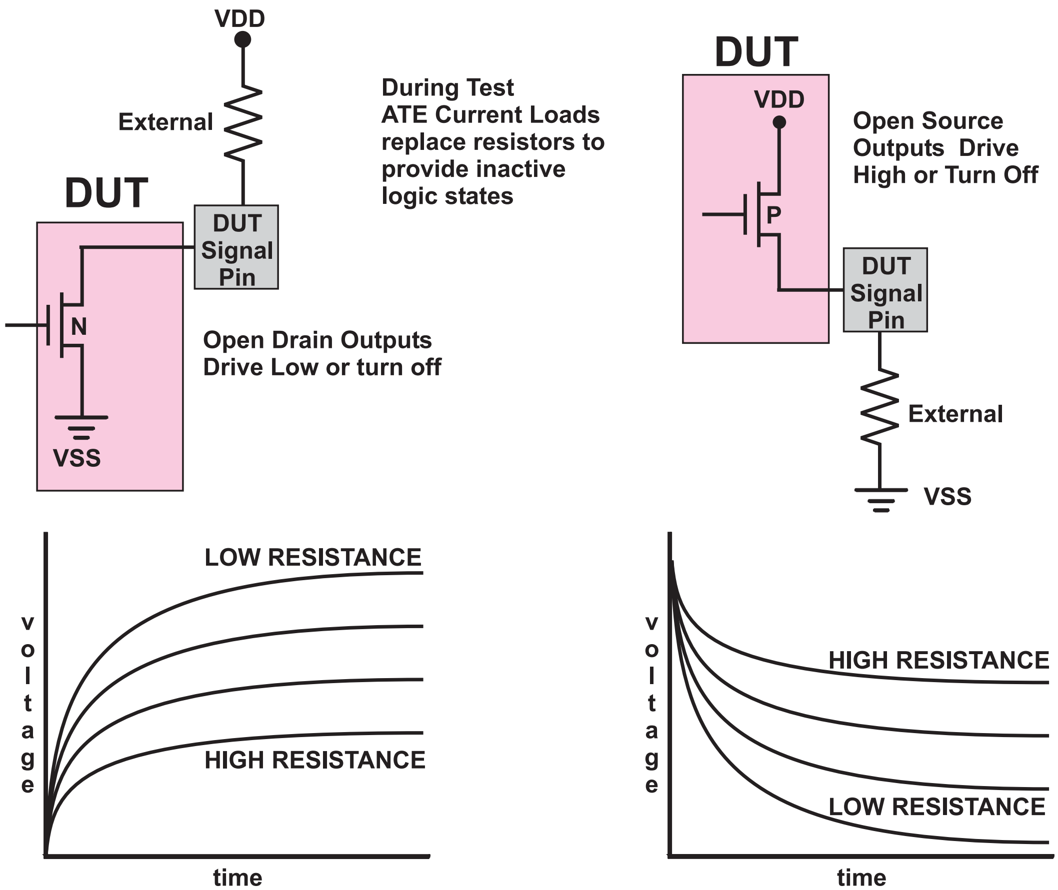


Figure 8-27 Open Drain and Open Source Outputs

When executing high speed functional tests, consideration must be given to the value of an external load resistor (or the current supplied by a current load). The time required for an open drain output signal to transition from a low to a high depends on the external load current and the associated capacitance. If too large a resistor (or too small a load current) is selected, the output may not reach its logic level soon enough to pass the functional test vector pattern.

These outputs can be sensitive to changes in test hardware. Different results may be experienced between wafer test, hand test, and auto handler test due to the different capacitive loads presented.

Note: Be aware that when functionally testing open drain outputs there will be a VOL specification, but not a VOH specification. This is due to the fact that the output drives low otherwise it shuts off. The output must be tested in the “on” state using the VOL limit, and it must also be tested in the “off” state. It is the test system that provides the “off-state” voltage via the Vref voltage of the current load. Consider setting the VOL comparator limit to the DC VOL specification and setting the VOH comparator to the VOL specification plus 100 mV. This will ensure that the device is in a valid low condition when it is on, and it will also ensure that the device is not in a valid low condition when it is off. The same thinking applies to the open source output, but the VOH specification will be defined, so set the VOL comparator to VOH minus 100 mV.

Open Drain / Open Source — Key Points

- May switch too slowly for high speed functional testing
- Outputs require current loads and reference voltage
- Output timings affected by external capacitive loading

Functional Test Review

1. If a device specification defines VDD as 3.3 V ± 5%, what would be the value of VDDmax?

2. If a device specification defines VDD as 1.8V ± 5%, what would be the value of VDD during the functional VOL/VOH test? Assume a typical specification.
   a) 1.80 V
   b) 1.89 V
   c) 1.98 V
   d) 1.71 V
   e) 1.71 V and 1.89 V

3. The VIL/VIH specifications are verified by executing:
   a) A DC test
   b) A Functional test
   c) An AC timings test
   d) None of the above

4. When a test is made to guarantee the VIL/VIH specification and a failure occurs, the failing pin (as seen on the failing datalog) will be:
   a) An input pin
   b) An output pin
   c) A power supply pin
   d) None of the above

5. If a VIH test is made with VIH set at 2.0 V and the result of the test is a failure, how could the voltage be changed in order to make the test pass?
   a) Lower the VIH voltage by 0.4 V
   b) Raise the VIH voltage to VDD
   c) Raise the VDD voltage by 0.4 V
   d) None of the above

6. When performing the VOL/IOL VOH/IOH test functionally, the comparators are set to the specified VOL/VOH levels and the dynamic (or resistive) current loads are used to supply IOL/IOH. When this test results in a pass condition, all four parameters (VOL/IOL VOH/IOH) are guaranteed to have met the device specification.
   a) True
   b) False

7. When debugging functional VOL/IOL VOH/IOH test failures, it may be necessary to increase the test period (slow the test frequency) and repeat the test in an attempt to verify correct operation of the VOL and VOH tests.
   a) True
   b) False

8. When performing the Z-State (high impedance) test as a functional test, some method of output loading must be used to provide an intermediate voltage level. This voltage level will be sensed by test comparators when the output pin enters a high impedance state. A correct value for the intermediate voltage level would be:
   a) VDD
   b) VSS
   c) (VOL+VOH)/2
   d) VOH
   e) None of the above

9. What is the purpose of performing a gross functional test?

10. What is the advantage of using equation based timing?

11. Open drain outputs do not have the ability to (choose the most correct answer):
    a) Drive a logic 0
    b) Drive a logic 1
    c) Source current
    d) B and C

12. What is the meaning of RO in the statement “The input control signal is in RO format.”?

13. Which signal format must be used to guarantee both setup and hold times?

14. When data changes only at T0, what is the signal format called?
    a) DNRZ
    b) RZ
    c) RO
    d) None of the above

15. Draw the wave shape for an SBC signal when the functional data is a logic 0?

16. What is the formula used to find the test cycle time when the operational frequency is known?

17. What is the advantage of performing a functional opens and shorts test rather than a DC opens and shorts test?

18. When performing a functional opens and shorts test current is forced by:
    a) The PMU.
    b) The programmable current loads.
    c) Voltage is forced, not current.
    d) None of the above.

19. A functional opens and shorts test uses the comparators in the Pin Electronics to detect open shorted conditions.
    a) True
    b) False