Soft Test

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DFT Fundamentals
1 Day Seminar

Today's Test and Product Engineers are regularly involved with DFT enabled chip designs, but the details of DFT test methodologies often remain a mystery. Design for Testability courses have been offered in the past, but most focus primarily on circuit design – not Test. This course has been developed specifically for engineers involved with component test of digital IC's.

DFT spans many disciplines and introduces terminology and concepts that are new. These issues are addressed as the course moves step-by-step through DFT Strategies, Circuit Implementation, Test Methodologies, and DFT ATE.

Fault Models, ATPG, Structural Test, Reduced Pin Count Test and Iddq are just some of the topics covered. The course material will enhance your current knowledge and you will likely find that you can put into practice what you learn immediately. This DFT Fundamentals Course is designed to provide a foundation of knowledge that will enable you to take full advantage of the benefits associated with DFT technology.

The Course
Lecture begins with a brief discussion of existing test issues and a first look at DFT. Next, Automatic Test Pattern Generation (ATPG) and Fault Models are covered. This provides the framework for understanding Scan Vector Patterns, Delay Tests, and Pattern debug.

DC and AC Scan are explained in detail, including DFT Structures, Test Strategies, and Timing Sequences. Boundary Scan 1149.1 (JTAG) is explained in similar detail followed by an in-depth discussion of Built-In Self Test (BIST) for Memory and Logic circuits.

The procedures and benefits of Reduced Pin Count Test are explored along with IOBIST. The course concludes with a comparison of DFT ATE to more traditional ATE. For more details of what is included in the course please see the attached Course Outline.

Who Should Attend
Test and Product Engineers, Engineering Managers, Sales Engineers, Field Service Engineers and Maintenance Technicians have all benefited from this course.

When, Where & Cost
Soft Test offers training services at our Sunnyvale CA facility on a regular basis and we also offer on-site training at your facility. Tuition is $495 per attendee and includes all course material. Give us a call for additional information and class schedules or visit our web site at **www.soft-test.com**

Class Registration
Registration is available on-line at our web site or contact the East Coast sales office at 386 478-1979. Email inquires to **admin@soft-test.com**

Summary
Test engineering is typically learned on the job, but in the case of DFT the more subtle issues are best addressed directly with lecture and examples. Get a head start now by attending our DFT-Test-Focused 2-day course.

There's More
Please visit our web site at for additional information and schedules for this course or download the "Quiz" and see if this course is right for you. Soft Test also offers technical training and publications for Digital Test, Mixed Signal Test, Memory Test and a variety of books and videos related to the semiconductor industry.

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DFT Fundamentals
1 Day Seminar

Course Length: 1 day

Purpose

This course is designed to explain the concepts and techniques associated with testing DFT enabled digital circuits. The information presented is founded upon DFT theory, but is also practical, relating directly to test problems, test programs and test equipment. The information presented will enable you to better understand how the various tests are implemented and how to verify and trouble-shoot problems.

Our Goal

Our goal is to provide useful information that will quickly improve the skill set required to be a productive digital DFT Test or Product Engineer. We present an environment where questions and interactions are welcomed and everyone is treated with respect regardless of their experience level.

Content

The course information presented includes the following:

- Introduction to DFT and current test issues
- Fault Models
- Automatic Test Pattern Generation (ATPG)
- DFT Details
- DC and AC Logic Scan
- Boundary Scan IEEE 1149.1 JTAG
- Built-In Self Test – Vector Compression - Iddq
- IO BIST and Reduced Pin Count Test
- DFT Focused ATE

Distribution Materials

Handout of course slides and all classroom materials are provided with the course

Prerequisites

Students should have completed the Soft Test *Digital Test Technology* class or have equivalent experience.

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Course Outline: DFT Fundamentals - 1 Day

Introduction – Test Problems
Expensive / Time Consuming / Complicated
Frequency / Pin Count / Accuracy
Problems -Design, Fabrication , Assembly, Reliability

Semiconductor Trends
Moore's Law / Frequency / Die Size / Cost / Functions
Transistor "Scaling" - trends and effects

Fault Models
Introduction - Behavioral Level / Gate Level (RTL) / Component Level
Types of Fault Models – examples detailed
(DC) Stuck-at
Opens
Bridging
Functional
Toggle
(AC) Transition Delay
Path Delay

Automatic Test Pattern Generation
What is ATPG?
Structural Test
Overview of the ATPG process
Targets - Cone of Logic
Injecting Faults
Generating Vectors – examples using various Fault Models
D and Dbar Notation
Sensitive Paths
Reconvergent Fanouts
Reconvergent Inputs
ATPG vector validation
Fault Coverage / Fault Grading

Design For Test (DFT) Introduction
Functional vs. Structural Test
Ad-Hoc vs. Structured DFT
DFT methods
Full Scan vs. Partial Scan
DFT benefits

DC Scan
Implementing Logic Scan
Flops – Mux-D

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ATPG and Scan Logic
Single, Multiple Chains
Scan Terminology
Scan Timing Diagrams – detailed waveforms, timing values, timing sequences
Shared Scan interface functions
Shifting Scan Data – what's important, ways shifting can fail
Testing Scan Logic – Scan integrity tests
Data Alignment Issues – examples, keeping it correct
Why DC Scan Tests Fail

AC Scan
Why perform AC Scan?
Delay Fault Models and AC Scan
Delay Path Distribution
Path Delay Example – Ideal Case
Transition Delay Example
Dynamic Hazards
Robust Delay Rules, Tests
AC Scan Terminology
Delay Test Examples
Strategies for Delay Tests

How AC Scan works
Launch On Shift (L-O-S)
LOS – detailed timing
LOS – test generation and associated issues
Functional Launch (Launch on Capture LOC)
Functional Launch – detailed timing
Functional Launch – test generation and associated issues
AC Scan Debug
Using AC Scan to make Timing Measurements
Clocks and Phase Lock Loops (PLL)
PLL basics / Chop Clocks

Boundary Scan 1149.1 IEEE Standard - JTAG
Introduction to Boundary Scan and the JTAG team
Why it was needed (PCB test requirements)
The IEEE 1149.1 Standard – what's defined
Boundary Scan Register functions
TAP Controller and dedicated pins
TAP 16 State Machine
TAP Operations
Boundary Scan Instructions
Instruction Behavior
Boundary Scan Register hardware
Bypass Register
Identification Register
BS Timing – Instruction Load
BS Timing – Data Scan
Using BS for parametric tests – VOLVOHVIL/VIH/IOZL/IOZH
Trouble-shooting with Boundary Scan
Testing the Boundary Scan hardware

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Built-In Self Test (BIST)
BIST defined
BIST applications
Memory BIST Architecture, Algorithms
Logic BIST Architecture
Pseudo-Random-Pattern-Generation (PRPG)
Linear Feedback Shift Register (LFSR)
LFSR designs: Type 1 & 2, Pattern Sequences
Seed Codes, Polynomials
Correlated Data Issues
Phase Shifters, Spreaders, Broadcasters
Output Compression – Multiple Input Shift Registers (MISR)
Output Signature
Logic BIST Test Sequence
BIST Clocking

IO BIST – Reduced Pin Count Testing (RPCT)
Why IO BIST
Reduced Pin Count Testing, what's involved
IO BIST pin circuitry
No Contact Shorts Test
Basic IO Functional Test (VOL/VOH/VIL/VIH) – no contact
IIL/IIH No Contact Leakage Tests

DFT and ATE systems (1 hour)
ATE system overview – types of test systems
Uses for each type of system
Introduction to DFT ATE

DFT Summary

Q & A

Total Number Correct

____

Design for Test (DFT) - *Training Evaluation*

Name: ______________________________ Date: ______________________

Match the terms with the definitions below.

A: MISR (acronym))	F: Compression	K: Bypass	P: MBIST (acronym)
B: Oppressor	G: Fault Coverage	L: Data Rotators	Q: BIST (acronym)
C: ATPG (acronym)	H: Reset	M: Fault Model	R: Spreader
D: AC Scan Model	I: Flush Tests	N: PRPG (acronym)	
E: Transition Delay	J: Output Signature	O: Seed Code	

_______ 1) The term that describes the behavior of a defective circuit based upon a specific type of defect

_______ 2) The process of generating test vectors for digital logic using algorithmic based software tools

_______ 3) A type of fault model that targets a single gate that is "Slow to Rise" or "Slow to Fall"

_______ 4) A term used to describe how effective a vector pattern is at detecting and screening out devices that contain faults

_______ 5) Often referred to as Scan Integrity tests, these vectors verify that the Scan chains work properly. They are normally the first Scan tests within a Scan Test Sequence.

_______ 6) One of the mandatory IEEE 1149.1 Boundary Scan instructions

_______ 7) Test logic contained within the circuit, which generates the input stimulus and captures the output response for testing all or part of a circuit design

_______ 8) Phase Shifter circuits, made using XOR gates, generate rotations in the data produced by the Pseudo-Random Pattern Generator. What is another name for this type of circuit?

_______ 9) The type of circuit generally used for Output Compression in BIST logic

_______ 10) This term referrers to the final compressed test result stored in the MISR, often shifted out to the ATE system for evaluation

Continue

Select the correct answer for the questions below.

11) Fault Models are built upon circuit abstraction, the highest level of circuit abstraction is:
a. Behavioral Level
b. Gate Level
c. Component Level

12) All IEEE 1149.1 Boundary Scan architectures must incorporate the use of a 24 state machine:
a. True
b. False

13) The Bridge Fault Model works on the assumption that one or more circuit nodes are open:
a. True
b. False

14) In order for ATPG tools to work effectively, the circuit must be:
a. Highly Controllable
b. Highly Observable
c. Mostly combinational logic (limited sequential logic)
d. All of the above

15) "TRST" Test Reset is one of the five mandatory pins associated with the IEEE 1149.1 TAP Controller interface:
c. True
d. False

16) Scan is a design technique that converts sequential logic to combinational logic, enabling ATPG tools to work effectively. This is accomplished by:
a. Converting Normal Flip-Flops to Scan Flops, then chaining the flops together
b. Adding specialized DFT circuitry which converts Normal Flops to XOR gates, then chaining the gates together
c. Converting sequential logic to LFSR (input) and MISR (output) registers

17) During Scan test, the data shift speed should be:
a. 50MHz maximum
b. At-Speed (the operating speed of the device, or slightly higher if guardbanding)
c. A safe speed
d. 20MHz maximum

18) When implementing an AC Scan test the ideal condition is to set all "Off-Path" signal levels at:
a. Enabling Levels
b. Controlling Levels
c. Quite (calm) Levels
d. Logic One level

19) Functional Launch (LOC) is a Scan test technique that requires two functional clock cycles. Launch on Shift (LOS) is a Scan test technique that requires:
a. No functional clock cycles
b. One functional clock cycle
c. Two functional clock cycles
d. Three functional clock cycles

20) Iddq is a defect based test, the "q" stands for:
a. Quality
b. Quick
c. Quiescent

Answers at: http://www.soft-test.com/DFT/answers.htm