Testing A/D Converters – A Practical Approach

The seminar entitled "Testing Analog-to-Digital Converters – A Practical Approach" is a one-day information intensive course, designed to address the real life issues associated with testing A/D converters. The skills and knowledge acquired in this course extend well beyond A/D converters to provide a functional model for testing a variety of mixed signal circuits.

Today many Test, Product, and Applications Engineers are familiar with digital circuits but lack experience with mixed signal devices and modern mixed signal ATE equipment. This course explains the finer points of device specifications, ATE instrumentation, test methodologies, and techniques for avoiding common problems associated with testing today's complex devices. It is no longer necessary to attend the costly and time consuming "*University of Trial and Error*" - now you can quickly gain the practical knowledge you need directly from the experts.

In this seminar you will learn

- How ADC performance is validated
- ATE architectures for mixed signal testing
- How ADCs work, including five different device architectures
- ADC static linearity measurement specifications and specsmanship
- Three different measurement techniques for linearity
- ENOBs and Histograms
- ADC Dynamic Specifications
- Frequency Domain analysis of dynamic ADC performance
- AC timing parameters
- Test Engineering Tricks and Techniques for solving difficult challenges

Give us a call to schedule an on site class or visit our web site at www.soft-test.com for a schedule of current classes

Prerequisites

Due to the fast-pace of this course attendees must have a basic understanding of DSP and sampling theory. The Soft Test "Fundamentals of Mixed Signal Testing" course is a recommended prerequisite

Distribution Material

Power point presentation in "notes" format, over 175 slides

Tuition

The cost to attend this one-day course is $499.00 US, per attendee and includes all course material

Summary

Mixed Signal Testing requires knowledge of analog circuits, digital signal processing, sampling theory and mathematics, in addition to the traditional digital test issues. This tutorial cuts through the confusion and gives the attendee a jump-start in making the transition to mixed signal test engineering. Unlike many "theory based" tutorials this course is designed for the "hands on" engineer who needs to understand the practical issues of A/D testing.

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Course Syllabus

Conversion Basics –
- Digital vs. Analog Testing
- Mixed Signal Testing
- Converter Test Overview
- Verifying Converter Performance
- Static Testing
- Dynamic Testing

ATE Architectures for ADC Test –
- Traditional Linear ATE Architectures
- ATE Mixed Signal Architectures
- Waveform Generator Overview
- Waveform Generator Memory and Conversion
- Waveform Generator Conditioning and Filtering
- Waveform Digitizer Overview
- Waveform Digitizer Conditioning and Filtering
- Waveform Digitizer Capturing, Converting, and Storing
- Digital Signal Capture
- Digital Signal Processor
- DSP Library

ADC Theory of Operation –
- High Bandwidth Analog Input
- Quantization
- Quantization Error
- Clock
- Latched or Buffered Outputs
- Serial or Parallel Outputs
- ADC Block Diagram

Five Different ADC Architectures –
- ADC Technologies
- Flash
  - Decoder
  - Flash Example
  - Flash Advantages & Disadvantages
- Successive Approximation (SAR)
  - SAR Example
  - SAR Advantages & Disadvantages
- Subranging (Pipelined)
  - Subranging Advantages & Disadvantages
- Integrating
  - Integrator Timing
- Integrating Advantages & Disadvantages
- Delta-Sigma
- Sigma-Delta Advantages & Disadvantages

ADC Static Testing –

- ADC Static Terminology
  - Transition Voltages (V_T)
  - Code Width (CW)
  - Code Width of First and Last Codes
  - Full Scale Transition Range (FSTR)
  - LSB_{DUT} Calculation
  - Full Scale Range
- ADC Static Specifications
  - Offset Voltage and Offset Error
  - Gain Voltage and Gain Error
  - Differential nonlinearity (DNL)
  - DNL Example
  - No missing codes
  - Integral nonlinearity (INL)
  - "Center of Code"
  - INL Example – Code Centers
  - INL Example – Summation
- Comparison of INL Techniques
- Which is Best?
- Summary of ADC Static Specifications
- ATE Configuration for Static Test
- Example ADC Static Specification
- Parameter Measurement Requirements
- Which Codes to test?
- How to Test ADC Static Specs
  - Five Steps to Success With Static Tests
  - Providing an Accurate V_{ref}
  - Providing an Accurate V_{in}
  - Digital Stimulus
  - Digital Capture
  - Analysis Routines for Calculating Static Test Results
- Servo Loop Transition Voltages
- AWG Ramp Transition Voltages
- Test Implications
- Histograms
  - Calculating Histogram Parameters
  - Input Signal Overdrive
  - Average Hits per Code - Example
  - Histogram Example
  - Getting Gain and Offset from a Histogram
  - Problems with Histograms
- Segmented Ramp Technique
- Architecture-Specific Test Considerations
  - Flash Test Considerations
  - SAR Test Considerations
  - Subranging Test Considerations
  - Integrating Test Considerations
  - Sigma-Delta Test Considerations
  - Test Considerations Summary
- Static Testing Key Points

ADC Dynamic Parameters –

- ADC Dynamic Testing
- Signal Classification
- Harmonic Distortion
  - Frequency Domain Analysis
  - Distortion in the Frequency Domain
  - Total Harmonic Distortion
- Noise
  - Gaussian Noise
  - Quantization Noise
  - Correlated Noise
  - Noise in the Frequency Domain
  - Signal-to-Noise Ratio
  - Signal-to-Noise-and-Distortion
- Superposition in Linear Systems
- Intermodulation Distortion
  - IM in the Frequency Domain
- Intermodulation Distortion Testing
- Dynamic Range
- Spurs in the Frequency Domain
- Spurious Free Dynamic Range
- Testing ADC Dynamic Parameters
- Test System Configuration
- Example ADC Dynamic Specification
- Parameter Measurement Requirements
- Dynamic Test Checklist
  - AWG Coherent Sine
  - Reconstruction Filtering
  - Purifying Filter
  - Scaling the Input Signal
  - Level Shifting
  - Buffering the ADC Input
- Sampling Parameters for the Input Signal
- Coherent Sampling Example
- Digital Capture Instrument
- Analysis of Captured Data
- Other Dynamic Test Considerations
- Undersampling
  - Undersampling Equation
  - Undersampling Example
- Sparkle Codes
- Sine Histograms
- Sine PDF Math
- Sine Histogram Scaling to DUT
- Effective Number of Bits (ENOB)
- Effect of Jitter on ADC Results
- ADC Jitter Example

Dynamic Testing – Key Points

Summary – Questions and Answers

Testing ADC Knowledge Evaluation

If you miss more than 3, you are a good candidate for the One Day ADC Tutorial

1. How many measurable code widths does a 10-bit ADC have?
    a. 1024
    b. 1023
    c. 1022
    d. 1021

2. Which type of ADC requires a sample-and-hold circuit at its input?
    a. SAR
    b. Flash
    c. Sigma-Delta
    d. Pipelined

3. Which ADC parameter does quantization error affect most?
    a. Total Harmonic Distortion
    b. Signal-to-Noise Ratio
    c. Gain
    d. Spurious-Free Dynamic Range

4. Noise shaping is:
    a. An effect seen with flash ADCs
    b. An effect seen with SAR ADCs
    c. An effect seen with all types of ADCs
    d. An effect seen with sigma-delta ADCs

5. If an ADC has “no missing codes”, its DNL is guaranteed better than:
    a. ±0.5 LSB
    b. ±1.0 LSB
    c. ±1.5 LSB
    d. ±2.0 LSB

6. What advantage does a servo loop have over a ramp generarator for ADC linearity testing?
    a. It is a faster method
    b. It requires no special hardware
    c. It is a more accurate method
    d. It produces a lower distortion sinusoid

7. What is the primary disadvantge of using the normal histogram method for ADC linearity testing?
    a. It does not find DNL values
    b. It does not find sparkle codes
    c. It does not find INL values
    d. It does not find THD values

8. Which formula best describes the frequencies at which Intermodulation Distortion appears?
    a. $m * F_1 \pm n * F_2$
    b. $F_1 \pm F_2$
    c. $m * F_1 + n * F_2$
    d. $F_1 \pm n * F_2$

9. What is the "Effective Number of Bits" for an ADC?
    a. The resolution of the device
    b. The resolution of the device minus its measured INL value
    c. A calculation that relates SNR and linearity
    d. A measurement that relates THD and linearity

10. What is the dynamic range of a 16-bit ADC?
    a. 32dB
    b. 65535dB
    c. 16dB
    d. 96dB

To check your answers please visit our web site – the direct link is

http://www.soft-test.com/adc_answerkey.html