Memory Test Methodology

Course Information

This two-day course focuses on the fundamentals of Algorithmic Test Patterns and their use for fault detection within memory devices. The ability of each unique pattern to detect Specific Fault Types and the advantages and disadvantages associated with each pattern are discussed in detail. To simplify the complexities associated with various Algorithmic Test Patterns, a Static RAM is used as the primary test circuit throughout this course.

The following information accompanies the explanation of each algorithmic pattern:

* A flow chart
* Sample code used to generate the pattern
* Animated graphics to illustrate the relationship between address and data
* The unique fault coverage
* A formula for calculating the pattern's execution time

The Architecture and Performance Specifications of a typical Memory Test System are presented with emphasis placed on test system Options, their Value and Use.

Examples of Memory Test System Features and Options covered in this course are:

* Topological scrambling (address and data)
* Error catch (as used for Bitmaps and Redundancy Repair and Analysis)
* Clocked high voltage levels – VIHH & VBUMP
* Stored patterns – the memory version of vectors
* Timers and their use
* Parallel test

Goals:

The information presented will provide:

* An understanding of basic Memory Device Architecture
* An understanding of ATE Memory Test System Architecture and Options
* Methods of detecting various faults within memory devices
* Tips for producing quality Test Programs with maximum throughput

Content:

* Basics of functional memory testing using ATE (automated test equipment)
* Developing and using Algorithmic Patterns (software code examples)
* Debug and trouble shooting techniques

Who Should Attend

This course is designed to present the fundamentals of Memory Component Test for Test and Product engineers who are new to the field of Memory Test. Upon completion of this course the attendees will understand Algorithmic Test Patterns, how they are created and how they are used. They will have also gained an understanding of Memory Test System Architecture, their options and use.

When & Where

Classes are held at various locations on a regular basis. Give us a call to schedule an on site class or click here for the latest class schedule.

Soft Test Inc. Phone 386 478-1979 Fax 386 478-1760

The Cost
Tuition to attend this two-day course is $795.00 US, per attendee and includes all course material.

Class Registration
Contact the sales office at 386.478.1979 or register on-line at www.soft-test.com. Email inquires to admin@soft-test.com.

Distribution Materials:
Fundamentals of Memory Testing text and all class materials.

Prerequisites:
Attendees must have an understanding of logic devices, basic test methodologies and a fundamental understanding of ATE equipment. Soft Test's Digital Test Methodology class is a recommended prerequisite.

There's More
Please visit our web site at **www.soft-test.com** for additional information on this course. Soft Test also offers technical training and publications for Digital Test, Mixed Signal Test, Memory Test and a variety of subjects related to the semiconductor industry.

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Course Description

Course Length:
2 days

Purpose:
This course presents the Fundamentals of Memory Component Test using ATE for Test, Product and Applications Engineers. The course content focuses on algorithmic patterns and their use for fault detection within memory devices. The ability of each unique pattern to detect Specific Fault Types and the advantages and disadvantages associated with each pattern are discussed.

Goals:
The information presented will provide:

* An understanding of device specifications and functions of memory chips
* An understanding of ATE Memory Test System Specifications and Functionality Methods of detecting various faults within memory devices
* Methods of producing quality test programs with maximum throughput

Content:

* Functional testing and device specifications are explained in detail
* Developing and using Algorithmic Patterns (software code examples)
* Test program generation
* Using Test System Tools for analysis (Bit Maps, Shmoo, Search, etc)
* Debug and trouble shooting techniques

Distribution Materials:
Memory Test Methodology reference manual and all class supplies.

Prerequisites:
Attendees must have an understanding of logic devices, device specifications and test methodologies. The Digital Test Methodology class is a recommended prerequisite.

Memory Test Methodology

Course Syllabus

SRAM block diagram
- The workings of a Memory Cell
- SRAM is often a Flip-Flop

Array
- Stuck At Fault / What is it?
- What makes this fault occur?
- What will it look like to the end user?
- Under a SEM
- Coupling Fault
- Neighborhood Pattern Sensitive Fault

Addressing
- Row decoders
- Column decoders
- Addressing Faults

Data In/Out
- Output buffers
- Sense amps
- Transition Fault

Control Signals
- Chip Enable
- Stand-by power levels on SRAM
- Output enable
- Write enable
- Logic table review of data sheet

Patterns
- Checkerboard
  - Slides / Faults / Micro-code Examples / Test times
- Address complement
  - Slides / Faults / Micro-code Examples / Test times
- March
  - Slides / Faults / Micro-code Examples / Test times
- Read Modify Write timing and pattern
  - Slides / Faults / Micro-code Examples / Test times
- March C
  - Slides / Faults / Micro-code Examples / Test times
  - How is this different from March?
  - Where and why would it be used?
- Matts++
  - Slides / Faults / Micro-code Examples / Test times
  - How is this different from March?
  - Where and why would it be used?
- Sliding diagonal
  - Slides / Faults / Micro-code Examples / Test times
  - Where and why would it be used?

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Memory Testers and Options
Vectors and Micro-code
APG
Data Generator
Topological scrambling
- Address
- What is Topo scram on the DUT?
- What is scramble ram on the tester?
- What patterns will this affect?
- Data

Timer(s)
- Refresh
- Failure to program

Error Catch Ram
- Redundancy and repair
- Bitmap

Data RAM
- Vector type storage
- ROM's and OTP's
- User library

VIHH
- Special modes
- Programming of NVM's
- Software write protection in E2prom's

Vbump
- How and Why

Parallel Testing
- Resources per pin/site/tester
- Resources (some are options!) required per device to be tested
- DPS
- APG
- ECR
- Data Ram

Additional Patterns
- Walking 0/1's
  - Slides / Faults / Test times
- Galpat
  - Slides / Faults / Test times
- Butterfly
  - Slides / Faults / Test times
- Surround Disturb
  - Slides / Faults / Test times
- Moving Inversion
  - Slides / Faults / Test times

Class Summary
Q&A

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