

Digital Test Technology Knowledge Evaluation

If you miss more than 3, you are a good candidate for the Digital Test Technology class.

Name: _____ Date: _____

Match the terms with the definitions below.

A: Negative	F: Preconditioning	K: Boundary Scan	P: VOL	U: Fault Coverage
B: Static	G: Dynamic	L: Setup Time	Q: IOL	V: DPM
C: VREF or VCOM	H: VIL	M: Pin Electronics	R: VDDMAX	W: Fault
D: IDD or ICC	I: Binning	N: Comparators	S: Positive	X: DFT
E: IOH	J: Hold Time	O: Wafer Test	T: Defect	Y: Bi-directional or IO

- _____ 1) The parameter that defines the acceptable power supply current of a semiconductor device.
- _____ 2) This term indicates that the device under test is actively changing logic states.
- _____ 3) The AC parameter that defines the minimum amount of time that data must be held after a reference signal reaches a certain voltage point.
- _____ 4) A device pin that functions as an input, an output and is also capable of achieving a high impedance state.
- _____ 5) A term used to describe logic that is added to a circuit design to improve its testability.
- _____ 6) A means of categorizing or sorting tested devices into their appropriate groupings.
- _____ 7) The parameter that defines the minimum current that an output must source when driving a logic one.
- _____ 8) Circuitry located in the test head used to supply input signals to the device under test and to receive output signals from the device under test.
- _____ 9) The reference voltage associated with the dynamic current loads, used to control the switching point of IOL and IOH currents.
- _____ 10) The parameter that defines the maximum voltage which may be applied to an input pin when applying a logic zero.
- _____ 11) A physical flaw introduced into a circuit during the manufacturing process.
- _____ 12) The polarity of current when flowing into the test system.
- _____ 13) A measure of the effectiveness of a vector test pattern.
- _____ 14) The polarity of current supplied by the test system during an IOL test.
- _____ 15) The name of the IEEE 1149.1 standard

Continued

Select the correct answer for the questions below.

- 16) The VIL/VIH specifications are verified by executing:
- A DC test
 - A functional test
 - Only verified through Failure Analysis
 - No test, these parameters are guaranteed by design
- 17) Propagation measurements are only made at outputs:
- True
 - False
- 18) When performing a functional opens and shorts test, the current is forced by:
- The PMU
 - The programmable current loads
 - Voltage is normally forced, not current
 - None of the above
- 19) A linear search typically executes slower than a binary search
- True
 - False
- 20) When Performing the VOH test, the current forced during the test is:
- A positive current
 - A negative current
 - a or b
- 21) The IIL/IIH test verifies:
- Input capacitance
 - Input threshold levels
 - Input impedance
- 22) When the device specifications defines VDD as 3.0V +/- 5%, the value of VDDMIN is:
- 3.15 volts
 - 3.25olts
 - 2.85 volts
 - It depends on the technology
- 23) Open drain outputs do not have the ability to:
- Drive a logic 0
 - Drive a logic 1
 - Source current
 - B and C
- 24) The output enable parameter tests the transition time of an output changing from driving valid logic levels to a high impedance state.
- True
 - False
- 25) The first testing to take place on a new circuit design is often called:
- Quality Assurance Test
 - Design Validation
 - Class Test
 - Incoming Inspection