

## Design for Test (DFT) - *Training Evaluation*

Name: \_\_\_\_\_ Date: \_\_\_\_\_

Match the terms with the definitions below.

A: MISR (acronym)	F: Compression	K: Bypass	P: MBIST (acronym)
B: Oppressor	G: Fault Coverage	L: Data Rotators	Q: BIST (acronym)
C: ATPG (acronym)	H: Reset	M: Fault Model	R: Spreader
D: AC Scan Model	I: Flush Tests	N: PRPG (acronym)	
E: Transition Delay	J: Output Signature	O: Seed Code	

- \_\_\_\_\_ 1) The term that describes the behavior of a defective circuit based upon a specific type of defect
- \_\_\_\_\_ 2) The process of generating test vectors for digital logic using algorithmic based software tools
- \_\_\_\_\_ 3) A type of fault model that targets a single gate that is “Slow to Rise” or “Slow to Fall”
- \_\_\_\_\_ 4) A term used to describe how effective a vector pattern is at detecting and screening out devices that contain faults
- \_\_\_\_\_ 5) Often referred to as Scan Integrity tests, these vectors verify that the Scan chains work properly. They are normally the first Scan tests within a Scan Test Sequence.
- \_\_\_\_\_ 6) One of the mandatory IEEE 1149.1 Boundary Scan instructions
- \_\_\_\_\_ 7) Test logic contained within the circuit, which generates the input stimulus and captures the output response for testing all or part of a circuit design
- \_\_\_\_\_ 8) Phase Shifter circuits, made using XOR gates, generate rotations in the data produced by the Pseudo-Random Pattern Generator. What is another name for this type of circuit?
- \_\_\_\_\_ 9) The type of circuit generally used for Output Compression in BIST logic
- \_\_\_\_\_ 10) This term refers to the final compressed test result stored in the MISR, often shifted out to the ATE system for evaluation

*Continue*

Select the correct answer for the questions below.

- 11) Fault Models are built upon circuit abstraction, the highest level of circuit abstraction is:
- Behavioral Level
  - Gate Level
  - Component Level
- 12) All IEEE 1149.1 Boundary Scan architectures must incorporate the use of a 24 state machine:
- True
  - False
- 13) The Bridge Fault Model works on the assumption that one or more circuit nodes are open:
- True
  - False
- 14) In order for ATPG tools to work effectively, the circuit must be:
- Highly Controllable
  - Highly Observable
  - Mostly combinational logic (limited sequential logic)
  - All of the above
- 15) "TRST" Test Reset is one of the five mandatory pins associated with the IEEE 1149.1 TAP Controller interface:
- True
  - False
- 16) Scan is a design technique that converts sequential logic to combinational logic, enabling ATPG tools to work effectively. This is accomplished by:
- Converting Normal Flip-Flops to Scan Flops, then chaining the flops together
  - Adding specialized DFT circuitry which converts Normal Flops to XOR gates, then chaining the gates together
  - Converting sequential logic to LFSR (input) and MISR (output) registers
- 17) During Scan test, the data shift speed should be:
- 50MHz maximum
  - At-Speed (the operating speed of the device, or slightly higher if guardbanding)
  - A safe speed
  - 20MHz maximum
- 18) When implementing an AC Scan test the ideal condition is to set all "Off-Path" signal levels at:
- Enabling Levels
  - Controlling Levels
  - Quite (calm) Levels
  - Logic One level
- 19) Functional Launch (LOC) is a Scan test technique that requires two functional clock cycles. Launch on Shift (LOS) is a Scan test technique that requires:
- No functional clock cycles
  - One functional clock cycle
  - Two functional clock cycles
  - Three functional clock cycles
- 20) Iddq is a defect based test, the "q" stands for:
- Quality
  - Quick
  - Quiescent

Answers at: <http://www.soft-test.com/dft/answers.htm>